RESEARCH ARTICLE OPEN ACCESS

FPGA Implementation of Low Power Multi- Channel Generalized PID Controller for Industrial Automation Applications

M. Indira [1], B. Swapna [2]
Department of Electrical Communication Engineering
JNTUH/ TKR College of Engineering and Technology
Hyderabad - India

ABSTRACT

Proportional-Integral-Derivative (PID) controllers are widely used in Industrial automation systems. They are usually implemented either in hardware using analog components or in software using computer-based systems. In industrial applications, PID controllers are the most important one to attain the desired control performance for its simple control structure and easily parameter tuning. Thus, regarding the design of universal control structure, PID controller is the most commonly used one. During the past years, FPGA applications in mechatronics, control and signal processing have been growing in relevance as an economic and reliable option made to fulfil the requirements of critical processes.

In the proposed work a multi-channel PID controller will be realized by Field Programmable Gate Arrays (FPGAs). Combining FPGA with ADC and DAC. The VHDL will be used for code development, simulation and synthesis. The hardware configuration with multichannel ADC and DAC along with FPGA will be implemented. To the work, the structure of the built system is going to be designed to only include one hardware PID controller, and by switching the analog input and output, the control board could realize four generalized PID controllers to fulfil a variety control demands. The PID controller will be implemented through low power look up table (LUT) approach.

Keywords :— PID controller, FPGA, ADC,DAC, XILINX,CHIPSCOPE

I. INTRODUCTION

This Paper Demonstrates A Multichannel Digital Proportional Integral Derivative (PID) Controller Of A Motor With Fan Load In One Channel And Of A Voltage Regulator Circuit With Varying Resistive Load In Another Channel.

The Controller Was Realized By Combining Field Programmable Gate Arrays (FPGAs) With Analog To Digital Converter And Digital To Analog Converter.

The Target FPGA Device Used In The Multichannel PID Controller For A Fan And Voltage Regulator Is Spartan-3 Manufactured By Xilinx. This Board, Provides All The Tools Required To Quickly Begin Designing And Verifying Spartan-3 Platform Designs, While The Implemented Modules Are Also Suited To Other High Density FPGAs

In this multichannel proportional integral derivative (PID) controller for a fan and voltage regulator the design of an efficient PID controller based on the look up table (LUT) scheme is implemented. The PID controller reduces the cost of the FPGA design by enabling the chip to accommodate more logic and arithmetic functions while requiring less power consumption. Also, due to the flexibility of using look-up tables in FPGAs, the design method can be used to implement other algorithms such as anti windup compensation or adaptive control schemes.

For the next generation of FPGAs, in which analog to digital (A/D) and digital to analog (D/A) converters are built into the chip, the proposed structure is more efficient in terms of hardware resources, power consumption and control performance when compared with the standard micro-controller IP cores. This is due to the fact that custom-made logic can generally perform the general purpose micro-controllers.

The multi- channel generalized (proportional integral derivative) PID controller was realized on a Spartan-3 Field programmable gate array (FPGA) to control D.C fan speed and for regulating the voltage of a voltage regulator circuit.

The controller was used to set and regulate the speed of a DC motor fitted with a fan. To demonstrate the multi-channel capability of the controller, a voltage regulator built using an Operational amplifier (OP-AMP) that delivers power to a load resistor was built. The proportional integral derivative (PID) channel output controlled the input voltage to the op-amp in response to variations in output voltage of the op-amp due to load changes.

The block diagram of overall implementation is shown in Fig

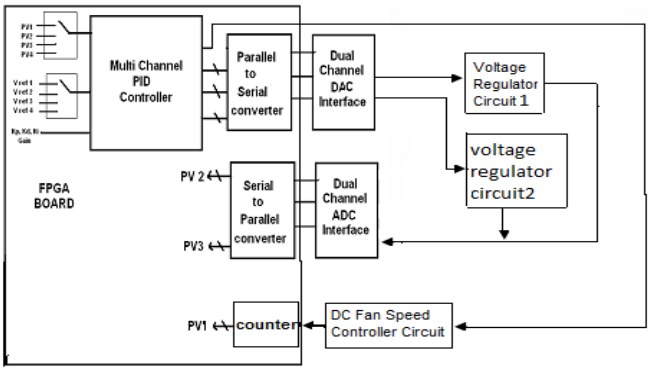

Fig.1 Multichannel Generalized PID Controller

The above figure shows three applications running in three different channels of FPGA based PID controller. The three applications are : Two voltage regulator circuits. One circuit maintains a constant voltage of 1V in one channel and other circuit maintains a constant voltage of 1.5v in another channel and the third circuit is of a DC fan speed controller

The same PID controller is used to control three applications simultaneously. PV is the process variable and V_{ref} is the reference value. Proportional, integral and derivative gains are given as input to the PID controller. As FPGA does not accept analog data Analog to Digital converter (ADC) is present. The accessory boards present external to the FPGA require analog data so Digital to Analog converter (DAC) is present. In DC fan speed controller circuit the rotations per second of the fan is maintained constant. This is accomplished by the PID controller by taking necessary control action. Voltage is maintained constant in the remaining two channels for this purpose an op-amp was used. The details of both the circuits are described in the later section.

II. IMPLEMENTATION

The schematic diagram of multichannel generalized proportional integral derivative(PID) controller of a DC motor with fan load in one channel and of a voltage regulator circuits with varying resistive loads in another two channels is shown in Fig

This paper demonstrate an Field programmable gate array (FPGA) industry grade multichannel proportional integral derivative (PID) controller featuring parallelism that affords the control of multiple loops. Reconfigurability is achieved through the use of generic style of coding.

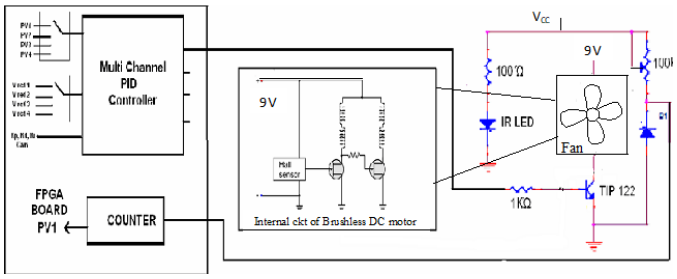

Fig .2 Schematic of multi-channel PID controller of a brushless DC motor with fan

Fig 2 shows the Hardware diagram of multi channel generalized PID controller with D.C fan speed controller circuit. It consists of DC motor operated fan speed controller circuit is interfaced to FPGA board. In this control section the speed of the fan is maintained constant. It consists of IR transmitter and Receiver to count the number of pulses of the DC fan. A TIP 122 transistor is used to provide the necessary drive required for the fan to rotate.

The speed of a fan driven by a DC motor is controlled by a pulse width modulated signal whose duty cycle can be controlled by a PWM signal from the PID controller. The PID controller selects the PWM word that generates a PWM wave (on time) and this is given to transistor that is in series with the DC motor. The speed of the dc motor with fan is monitored using an infrared transmitter and receiver. The infrared transmitter and receiver are mounted such that the infrared beam is broken by the blade of the fan. This generates the number of rotations of the DC fan which is fed to the FPGA dc motor control section.

The rotations per second (rps) is continuously compared with an internal reference and if a deviation occurs, an error signal is generated which changes the duty cycle such that the speed is regulated.

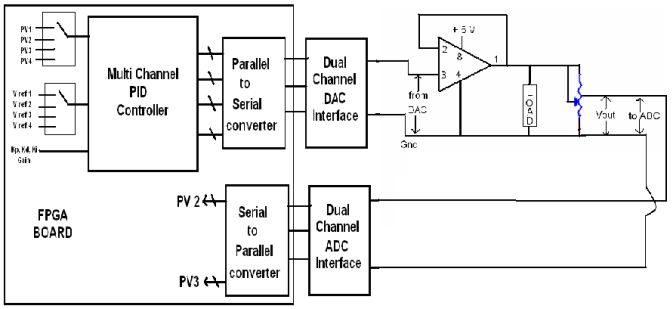

Fig.3 Schematic overview of multi-channel PID controller with voltage regulator circuit

Fig 3 shows the Hardware diagram of multi channel PID controller with voltage regulator circuit. Output is maintained constant at a particular voltage. An Op-amp is used to regulate

the voltage to a load resistor by signals from a DAC whose input is the output control signal from the PID controller. The op-amp used is an LM 358 connected as a voltage follower. The input voltage to the op-amp is the output of digital to analog converter.

The figure shows the schematic overview of a multi channel PID control of a circuit whose output is maintained constant. An OP-amp is used to regulate the voltage to a load resistor and is controlled by signals from a Digital to Analog

converter whose input is the output control signal from the PID controller. The voltage across the load is sampled using a potential divider and fed back via an Analog to Digital converter to the PID controller. The op amp is configured as a unity gain follower for the purpose of demonstration. ADC gives the voltage value to sample in which will be compared with the reference voltage and gives the error signal to the PID controller then it process the signal and generates the correction signal that will be given to DAC to maintain the voltage.

III. RESULTS

The rotations per second of the DC fan are observed in the chip scope tool of FPGA .The reference count is 300rps and the output is observed to vary between 296 rps and 309 rps. This slight variation is due to the power supply variations of the 12V power supply is provided to the DC fan motor.

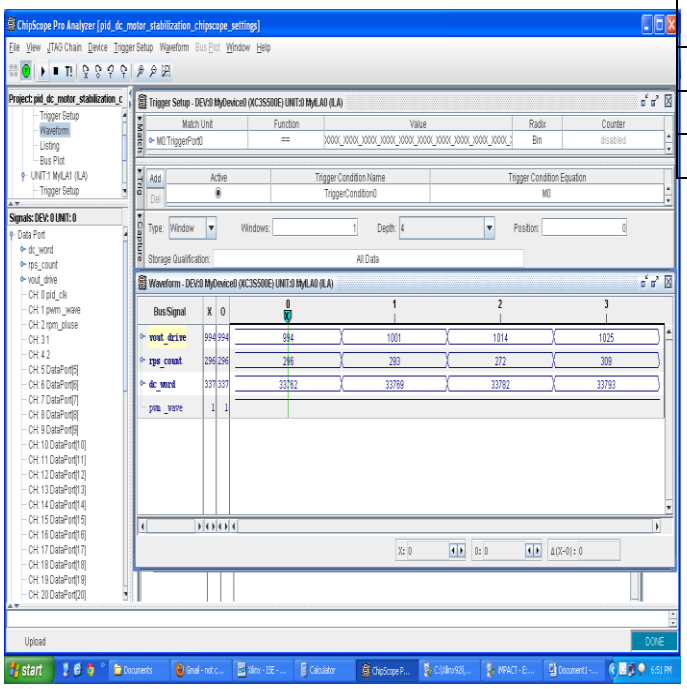

Fig.4 Chip scope results for DC fan

The results of DC fan motor control actions are shown in Table1.

Table 1. DC fan controller observations

S. No.	V_{out}_drive	Revolutions per second
1	994	296
2	1001	293
3	1014	272
4	1025	309

Voltage Regulator operation observations

The output of the op-amp LM358 at pin1 (across load) with voltmeter with load variation is shown in in tables 2 and 3.

Voltage regulator circuit I (Reference voltage is 1.5V)

Table 2. Output voltage of voltage regulator circuit I

S. No.	Load resistor value	Output voltage
1	40 ohm	1.47V
2	75 ohm	1.49V
3	100 ohm	1.5V

Voltage regulator circuit II (Reference voltage is 1V)

Table 3. Output voltage of Voltage regulator circuit II

S. No.	Load resistor value	Output voltage
1	40 ohm	0.99V
2	75 ohm	0.96V
3	100 ohm	1V

From the above observations it is seen that the PID controller is satisfactory in operation

1) for the dc motor with fan that maintains the speed constant within reasonable limits against power supply variations,
2) for the voltage regulator circuits that maintains the voltage constant within reasonable limits against variations in load current by varying the load resistance.

IV. CONCLUSION

Today's high-speed and high density FPGA provide viable design alternatives to ASIC and

microprocessor- based implementations. Implementing PID controllers on FPGAs features speed, accuracy, power, compactness and Reconfigurability.

A digital PID controller implemented in FPGA technology is a configurable controller in terms of latency, resolution and parallelism. High bit width controllers can easily be implemented in FPGA technology. The speed or execution or latency of the controller can be precisely controlled with amount of reuse arithmetic elements such as multiplier and adders.

V. FUTURE SCOPE

In future, with the PCI interface IP, An interface circuit to connect the PID controller command input and the host computer could be planned, and the user is going to easily modify the control parameters by manual or by some adaptive algorithm to improve the flexibility of the proposed hardware system.

REFERENCES

[1] Y.F. Chan, M. Moallem and W. Wang," Efficient implementation of PID control algorithm using FPGA technology," 43rd IEEE Conference on Decision and Control, vol. 5, pp. 14-17, Dec. 2004.

[2] Yuen Fong Chan, M. Moallem and Wei Wang, "Design and Implementation of Modular FPGA-Based PID controllers," IEEE transactions on industrial electronics, vol. 54, no. 4, pp. 1898-1906, Aug. 2007.

[3] Xilinx, "Spartan-3 FPGA Family: Complete Data Sheet"2004. http://www.xilinx.com/bvdocs/publications/ds099.pdf

[4] Digilent, Inc., "Digilent Spartan-3 System Board", June, 2004. http://www.digilentinc.com/Data/Products/S3BOARD/S3BOARD-brochure.pdf

[5] Jacob Millman, Christos "Integrated Electronics ", Tata MC Graw- Hill, 1991