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Harmonic Reduction of Cascaded H-Bridge Inverters with Photo VOLTIC By Considering DC Voltage Ratios and Device Loss

S. Manobalan[1], R.Anandaraj[2]
PG scholar [1], Associate professor [2]
Department of Electrical and Electronics Engineering (PED)
E.G.S.Pillay Engineering College Nagapattinam
TamilNadu-India

ABSTRACT
The main theme of this paper is the least possible of total harmonics reduction of the staircase modulated output voltage of single phase multilevel inverter with or without exclude of the lowest order hormonics. The slight THD (total harmonics distortion) values conjunction with the analogous step angle and dc voltage source ratio have been acquire for the 13 level cases. In the time of resistive load and inductive load consumed the power supply from the inverter considers device voltage drop like the slight WTHD (without total harmonics distortion) values conjunction. So mainly this paper is used for the hybrid power station and vehicles. The photo voltaic is used as renewable energy source another power supply is get from the battery.
Keywords:- VOLTIC, EMI, THD, DC, CHB

1. INTRODUCTION

In recent years high frequency switching converters applications in the dc power distribution are increasing. Particularly in the area of automotive systems, the main focus is on hybrid vehicles and power station. As the power conversion system is becoming miniaturized, increasing the power density is one of the challenging issues. Nowadays, switching mode converters with higher power density and low electromagnetic interference (EMI) is required. Several types of switch-mode dc-dc converters

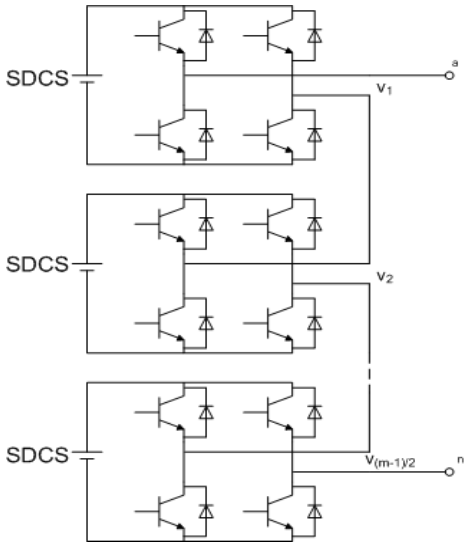
(SMDC), belongs to buck, boost and buck-boost topologies, have been developed and reported to meet variety of applications. Major concern in automotive and telecom power supply systems, is to meet the increased power demand and to reduce the burden on the primary energy source, i.e., built in battery or ac utility. This is possible by adding additional power sources in parallel to the existing battery source.

Modern power semiconductor devices have made the cascaded H-bridge multilevel converter, patented in **1975**, practical for use as medium/high-voltage inverters, medium-voltage industrial drives, static VAR compensators, etc. In general, multilevel inverters with various topologies have become increasingly popular due to their advantages of higher voltage capability, higher power quality, lower switching losses, and improved electromagnetic compatibility. In addition, the growing importance and availability of low-voltage dc sources such as photovoltaic arrays and fuel cell stacks further enhances the usefulness of these inverters to produce relatively large ac voltages from them without using transformers.

One advantage of the series H-bridge circuit over other multilevel topologies is that it is comprised of similar cells – leading to a modular design. The original series cascaded H-bridge inverter patent, and many succeeding studies, prescribed the same value of dc source voltage being applied to each cell. Later research has shown that the overall number of output voltage levels can be increased for a given number of semiconductor devices if a binary (1:2) ratio between the dc source voltage values is used, to achieve lower total harmonic distortion (THD). Output voltage distortion is a key issue in many inverter applications; e.g., as a motor drive, such distortion leads to undesirable machine heating and vibration/noise. Around the same time, the ternary (1:3) ratio was investigated and a patent obtained for general integer ratios between the dc source voltages of the H-bridge cells. Other binary and ternary source voltage ratio designs have been proposed, and another patent has been issued for these same integer ratios. For staircase modulation operation, Huang, and Jiang and Lipo, proposed using non-integer dc source voltage ratios for multilevel inverters to achieve minimal total harmonic distortion (THD) and frequency-weighted total harmonic distortion (WTHD), respectively, the latter being a more appropriate measure than THD for inductive load applications such as motor drives. But since the focus of was on three-phase applications, that work excluded the effect of the triple harmonics, which cannot be ignored for single-phase applications. Huang also considered the three-phase case; furthermore it was under the conditions of either constant-voltage (equal source) variable-angle or constant-angle (equal step interval) variable-voltage; the more general variable-voltage (unequal source) variable-angle results were not described therein. Also, calculation of line voltage THD in a cascaded H-bridge inverter with unequal voltage sources was presented.

II. CASCADE H-BRIDGE INVERTER MULTILEVEL INVERTER

The Cascaded H-Bridge (CHB) multilevel inverter is based on the series connection of single phase H-bridge inverters with separate DC sources. The topology is shown in Figure 2.1 the output phase voltage is synthesized by the addition of the voltages that are generated by different modules. If the separate DC sources have the same voltage level (Vdc), the resulting phase voltage will be able to range from −nVdc to nVdc which would have 2n + 1 levels. And n is the number of the total modules or the number of separate DC sources. As the number of DC sources increases, there would be more levels in the output voltage. So the output voltage waveform will be nearly sinusoidal, even without filtering.



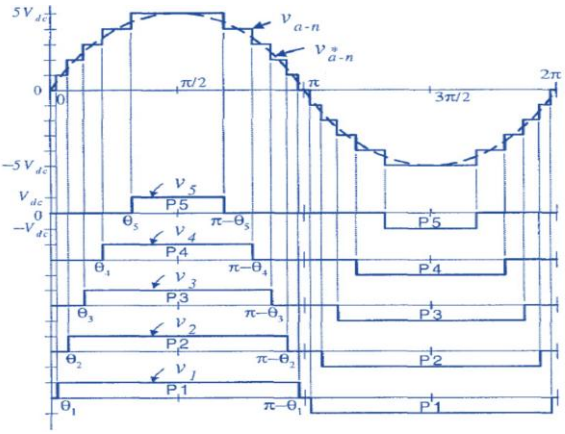
Cascade h-bridge multilevel inverter topology

The cascaded inverter topology has several advantages that have made it attractive in medium to high-power applications. The first one is its modularity. Each DC source is fed into an individual full bridge inverter so it is easy to plug into more separate DC sources without changing the dimension of the system. Moreover, the switching stress for each switch device would be less than the regular two level topology since the switch and diode need only withstand one separate DC voltage. If the Harmonic Selective Modulation method is used, the switching frequency will be at the fundamental frequency which decreases the switching loss. Finally, as mentioned above, the output voltage waveform is nearly sinusoidal which decrease the cost of the filter.

III. SELECTIVE HARMONIC ELIMINATION

The basic idea of the selective harmonic elimination is to pre-determine the switching angle for each module to get the expected waveform of the output. To explain its implementation in the cascaded H-bridge multilevel inverter, one example of five modules, eleven levels CHB multilevel inverter is shown in Figure 3.4. By using Fourier Transform, the output voltage V (ϕt) can be expressed as

$$V(\varphi t) = \frac{4vdc}{\pi} \sum_{n=1}^{\infty} [(\cos n\theta 1 + \cos n\theta 2) + \ldots + \cos n\theta 5)] \sin(\varphi t)$$



Output waveform of a 9-level cascade inverter

Where n is the harmonic order. Since the waveform is both half wave symmetry and odd symmetry, n = 1, 3, 5, 7...Usually, the normalized Fourier coefficients of the magnitude are used for further analysis. The normalized magnitude can be obtained by dividing Vdc on both sides of equation 3.1. Hence, the normalized Fourier coefficients for each harmonic order components are

$$H(n) = \frac{4}{\pi n} \sum_{n=1}^{\infty} [(\cos n\theta 1 + \cos n\theta 2) + \ldots + \cos n\theta 5)]$$

Where n = 1, 3, 5. . .Then by choosing the conducting angle $\theta 1$ to$\theta 5$ appropriately, it is possible to eliminate some target harmonic components. Another point need to be mentioned is that the number of harmonic components which can be eliminated by this modulation method is one less than the number of the conducting angles since one degree of freedom should be given to the fundamental components of the waveform. In this case, the number of harmonics that can be eliminated is 4. Since the triple harmonic would not exist in the line to line voltage, the 5th, 7th, 11th and 13th order harmonics are chosen as the target harmonics that need to be eliminated in this case. The following equation can be obtained:

$$\cos(5\theta_1) + \cos(5\theta 2) + \cos(5\theta_3) + \cos(5\theta_4) + \cos(5\theta_5) = 0$$
$$\cos(7\theta_1) + \cos(7\theta 2) + \cos(7\theta_3) + \cos(7\theta_4) + \cos(7\theta_5) = 0$$
$$\cos(11\theta_1) + \cos(11\theta 2) + \cos(11\theta_3) + \cos(11\theta_4) + \cos(11\theta_5) = 0$$

$cos(13\theta_1) + cos(13\theta 2) + cos(13\theta_3) + cos(13\theta_4) + cos(13\theta_5) = 0$

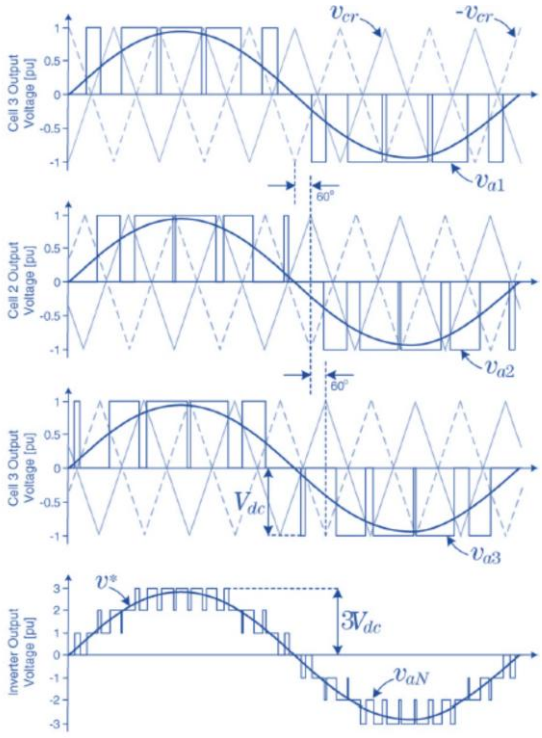
$cos(\theta_1) + cos(\theta 2) + cos(\theta_3) + cos(\theta_4) + cos(\theta_5) = 5mi$

Where mi is reference modulation index which is defined as mi = Vref/5Vdc

One advantage of this modulation method is that the inverter are switching at the fundamental frequency which decreases the switching losses. However, the pre-calculation of the conducting angle requires the solution of non-linear equation. When the level of inverter increases, the number of the non-linear equations would also be very high. Then the solution for these equations would be inaccurate which may increase the distortion in the output voltage waveform.

IV. PHASE SHIFTED PULSE WIDTH MODULATION

Phase shifted PWM is one of the most commonly used modulation method in CHB multilevel inverter since it is very suitable for the modularity of the topology. For each module, the reference signal is the same. However, the carrier waveform (usually triangular waveform) for each module would have a phase shift to ensure the step characteristic of the output voltage. How many degrees are the phase shift between each module depends on the modulation method for the individual H-bridge inverter. If the unipolar modulation method is selected, the phase shift between each module should be 180_/k to achieve the lowest output voltage distortion; if the bipolar modulation method is chosen, the phase shift between each module should be 360_/k, where k is the number of modules. Three modules, seven levels CHB multilevel inverter with unipolar modulation method is shown in Fig.



Three cell PS-PWM waveform generation

The output voltage of the inverter is as k times as the output voltage of each module which is one advantage of this modulation method since the switching devices need only withstand the voltage of their modules. Moreover, the frequency of the output voltage has k times as the switching frequency of each modules which is beneficial in reducing the conducting losses of the inverter.

V. TOPOLOGY AND OUTPUT WAVEFORMS

The familiar 2-cell series cascaded H-bridge inverter topology, which will be utilized as the basic circuit for developing the results herein in the interests of simplicity and clarity. However, the operating principles generalize apropos to n-cell series cascaded H-bridge inverters. Two examples of the 2-cell inverter's output waveform (under staircase control) are shown; when the two dc source voltages (E1 and E2) are equal (to E) and when they are unequal. For an output voltage waveform that is quarter-wave symmetric (as in Fig. 2) with s steps of generally unequal magnitudes Ei, i= 1, … ,s, for the s dc voltage sources, its Fourier series expansion is given by

$$vo(t) = \sum\{ V_h \sin(h\omega t) \}$$

h odd

$$V_h = 4/h\pi[E_1 \cos(h\theta_1) + E_2 \cos(h\theta_2) + \ldots + E_s \cos(h\theta_s)$$

where the θi, i= 1, … , s, are the angles at which the s steps within the first quarter of each waveform cycle occur. Alternately, by defining the ratios ρi= Ei/Es, we can describe the output voltage over its first quarter-cycle by the piecewise-constant expression

$$v_0(\theta_j \le \omega t \le \theta_{j+1}) \sum_{k=0}^{j} Ek = Es \sum_{k=0}^{j} \rho 0$$

Where $\theta 0 = 0$, E0 = 0, ρ0 = 0, and $\theta s+1 = \pi/2$ for step j = 0, s. This is illustrated by a sketch in Fig. 2.5 of a 3-cell (7- level) inverter's output waveform showing the step angle and voltage ratio parameters. The problem of synthesizing such a stepped waveform with a desired value of V1 (the fundamental component) with some of the higher harmonics possibly set equal to zero, is equivalent to choosing the source levels Ei, i= 1, s, and the step angles $0 \le \theta 1 < \theta 2 < \ldots < \theta s \le \pi/2$ such that

$$4/\pi \left[E_1 \cos(\theta_1) + E_2 \cos(\theta_2) + \ldots + E_s \cos(\theta_s) \right] = V_1$$

$$4/3\pi \left[E_1 \cos(3\theta_1) + E_2 \cos(3\theta_2) + \ldots + E_s \cos(3\theta_s) \right] = V_3$$

Next, applying the identities $\cos(3\theta) = 4\cos(\theta)3 - 3\cos(\theta)$, cos(5$\theta$) = ... , etc., as in [15, 17-20], and defining ci as cos(θi), transforms from a set of trigonometric equations to the set of multivariate polynomial equations

$$\sum \rho_i c_i = V1 / 4 Es/\pi = m1$$

$$i = 1, .. , s$$

$$\sum \rho_i c_i = \{ 4 ci^3 - 3 ci \} = m3$$

$$i = 1, .. , s$$

where m1 is defined as the modulation index of the fundamental component (with respect to Es), etc. This set of equations can now be solved exactly (to yield multiple solutions in general) using procedures based on either Grobner bases or resultant polynomials, as described in and using algorithms available in. Note that a necessary condition for the existence of nontrivial solutions to (2.13) & (2.14) is that the number of steps s per quarter cycle be greater than or equal to the number of constraint equations. Therefore, as has been typically advocated, s-1 of the lowest harmonics can be eliminated as one way to reduce the waveform's distortion.

To quantify waveform distortion, let the THD of the output voltage be defined (as is usual) as

$$\mathbf{THD} = \sqrt{\sum_{h=2}^{\infty} \frac{v_h^2}{v_1}}$$

To quantify waveform distortion in another way, let the frequency-weighted THD (WTHD) of the output voltage be defined (being more appropriate than THD for motor drive applications) as

$$\mathbf{WTHD} = \sqrt{\sum_{i=0}^{n} \frac{v_h}{h^2} \Big/ v_1}$$

For three-phase applications, the triple harmonics do not appear in the line-line voltages under balanced conditions, so (2.15) and (2.16) can be modified to exclude those harmonics as special cases. In the following, the minimal THD obtained when the lowest harmonics are eliminated is compared to the situation where those harmonics are not so constrained. A similar comparison is made for minimal WTHD.

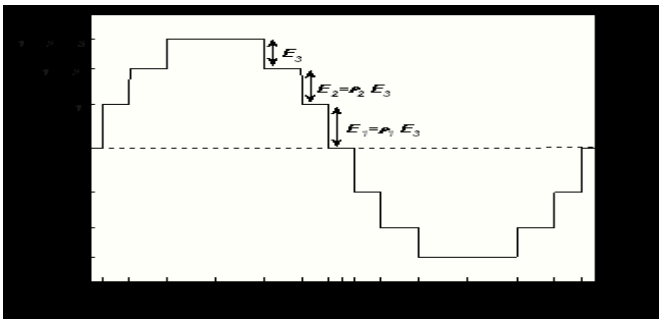


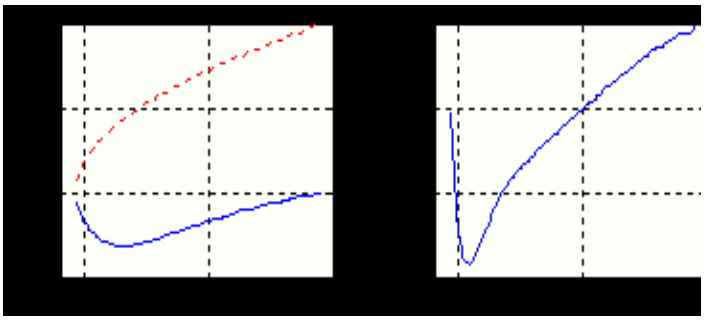
Fig. 3.2 A 3-step (7-level) waveform defined by its step angle and voltage ratio parameters.

VI. THE 7-LEVEL AND 9-LEVEL WAVEFORMS HARMONIC ELIMINATION

For the 7-level output voltage case with s = 3 steps per quarter cycle, analysis of was performed to solve for the step-anglesθ1 ,2, θ3 and ratios ρ1 ρ2, (with ρ3= 1) yielding the minimal THD for each m1, with m3 = m5 = 0 to eliminate the 3rd and 5th harmonics. This was followed by a similar analysis for the 9-level output voltage case to find the step-anglesθ1 , θ2, θ3,θ4 and ratios ρ1 ρ2 ρ3 (with ρ4 = 1) yielding the minimal THD for each m1, with m3 = m5 = m7 = 0 to eliminate the 3rd, 5th and 7th harmonics. The required voltage ratios and step-angles yielding the minimal THD for any m1 – with elimination of the lowest harmonics – are presented.

THD OPTIMIZATION

Without the HE requirement, the required voltage ratios and step-angles that would yield the minimal THD for the equal 7-level and unequal 7-level waveform cases were determined. Similarly this was also done for the equal 9-level and unequal 9-level waveform cases. The obtained minimal THD values are tabulated in Table I as are the corresponding required voltage ratios and step-angles.

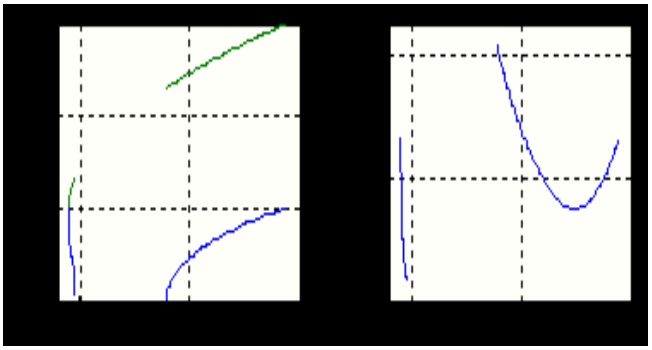


step angle solutions for varying $\rho_{1,1}$ ((b) Corresponding THD for varying $\rho_{1,}\theta_1$

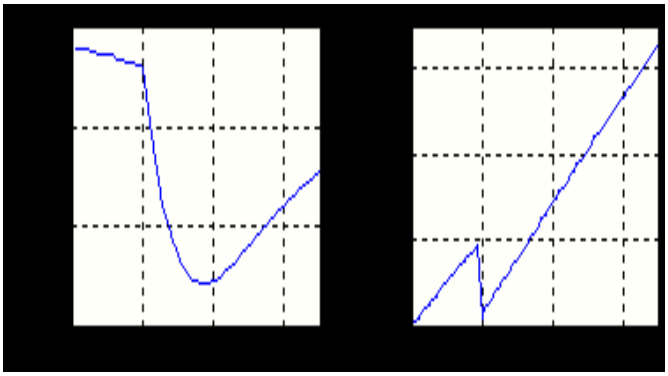
VII. WTHD OPTIMIZATION

With and without the HE requirement, the required voltage ratios and step-angles that would yield the minimal WTHD for the equal and unequal 7-level waveform cases, and the equal 9-level and unequal 9-level waveform cases, were determined. The obtained minimal WTHD values are tabulated in Table 5.2 as are the corresponding required voltage ratios and step-angles. It was noted that a WTHD < 0.5%, which was the performance target, was attained by the 9-level waveform so waveforms with more levels were not studied for further WTHD reduction.

Step-angle solutions for varying ρ1Corresponding WTHD for varying ρ1

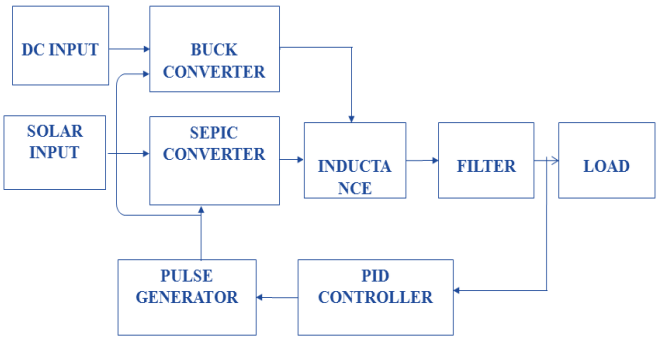


Minimum WTHD, and Fig3.5 (b) corresponding optimal ρ1 versus m1; harmonic eliminating case.



VIII. BLOCK DIAGRAM OF PROPOSED SYSTEM

The block diagram of proposed system consists of Buck converter, SEPIC converter, DC input, solar input, inductance, filter, pulse generator PID controller and load. Here, the function of SEPIC converter is to extract power from the solar input and feed into load, while the remaining load power demand is supplied by the dc source through buck converter.

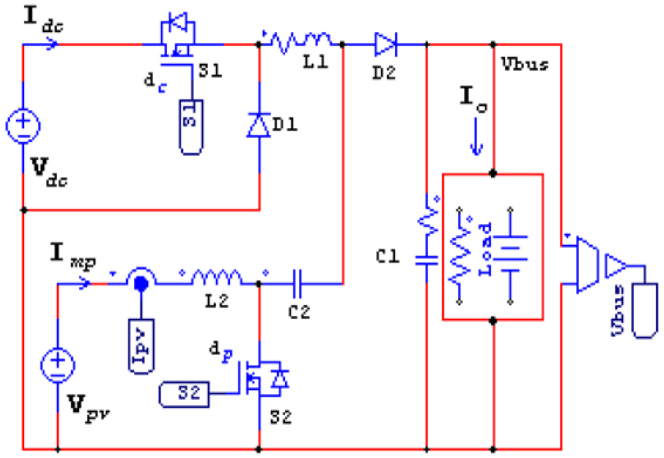


8.1 Block Diagram of Proposed System

DC input is given to the buck converter and solar input is given to the SEPIC converter. Buck and SEPIC converter is integrated by means of inductance. Because of this integration, only one inductor is sufficient enough on load side for performing the power conversion in both buck and SEPIC converter. Filter is used to remove the unwanted signals and harmonics. PID Controller will generate the triggering pulses. Resistive load is used.

8.2 Circuit Diagram

The circuit diagram of proposed system is shown. The diode 'D2' is common to both the converters, while the individual converters are having their own switching devices. Load and its filtering capacitor are common to both the converters. Hence the filtering requirement is less as compared to the individual converter connecting in parallel.

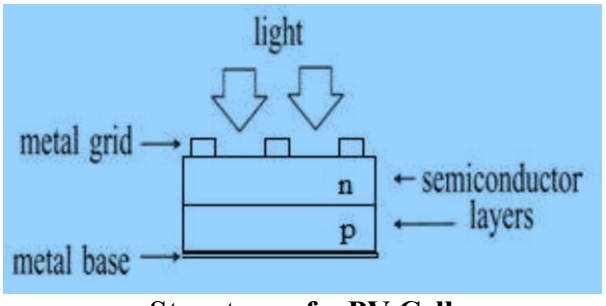


Circuit Diagram Of Proposed System

The buck converter is formed by: S1, D1, L1, R, while the SEPIC converter is formed by: S2, D2, L1, L2, C2, R.Depending on the location of the PV renewable energy source and dc-battery in the two input converter, there are two different power conversion combinations are possible.The main advantage of this integrated topology over the integrated topologies parallel connection at the load terminals is that the order of the power conversion topology is less by one. In view of order reduction the dynamical behaviour is somewhat simpler than when it is using two separate inductors. The circuit can actually operate either in continuous or discontinuous inductor current mode. But, its operation in a discontinuous mode of operation will not provide benefits for the power conversion, and also on the account of higher power demand the current flows in 'L1' for most loading conditions. Furthermore, 'L2' is designed such that current is continuous even at lower solar isolations. Here, the converter switching frequency must be chosen such that the current in 'L2' is continuous even at lower solar isolations. In view of this the circuit operation is discussed here only for continuous inductor current mode (CICM).

8.3 SOLAR PV MODULE

Renewable energy resources will be an increasingly important part of power generation in the new millennium. Photovoltaic systems produce DC electricity when sunlight shines on the PV array without any emissions. Structure of a solar cell is given below.

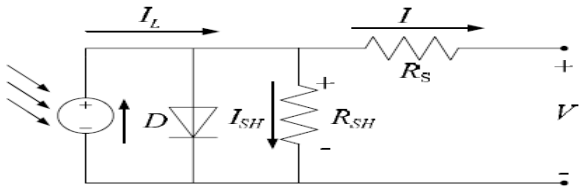


Structure of a PV Cell

A solar cell consists of a p-n junction fabricated in a thin wafer or layer of semiconductor (usually silicon). In the dark, the I-V output characteristic of a solar cell has an exponential characteristic similar to that of a diode. When solar energy (Photons) hits the solar cell, with energy greater than band gap energy of the semiconductor, electrons are knocked loose from the atoms in the material, creating electron-hole pairs. These carriers are swept apart under the influence of the internal electric fields of the p-n junction and create a current proportional to the incident radiation. When the cell is short circuited, this current flows in the external circuit; when open circuited, this current is shunted internally by the intrinsic p-n junction diode. The characteristics of this diode therefore set the open circuit voltage characteristics of the cell.

EQUIVALENT CIRCUIT OF THE PV CELL

The simplest equivalent circuit of a solar cell is a current source in anti-parallel with a diode. When exposed to light, a dc current is generated. The generated current varies linearly with the solar irradiance.

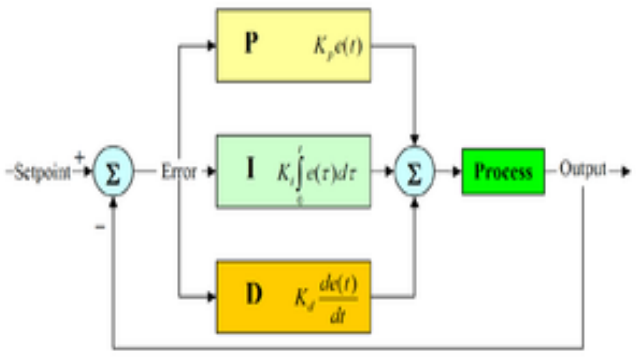


Equivalent Circuit of a PV Cell

The standard equivalent circuit of the PV cell is shown in the figure.

PID CONTROLLER

A proportional–integral–derivative controller (PID controller) is a generic control loop feedback mechanism (controller) widely used in industrial control systems – a PID is the most commonly used feedback controller. A PID controller calculates an "error" value as the difference between a measured process variable and a desired set point. The controller attempts to minimize the error by adjusting the process control inputs.



Block diagram of a PID Controller

The PID controller calculation (algorithm) involves three separate constant parameters, and is accordingly sometimes called three-term control: the proportional, the integral and derivative values, denoted P,I, and D. Heuristically, these values can be interpreted in terms of time: P depends on the present error, I on the accumulation of past errors, and D is a prediction of future errors, based on current rate of change. The weighted sum of these three actions is used to adjust the process via a control element such as the position of a control valve, or the power supplied to a heating element.

In the absence of knowledge of the underlying process, a PID controller is the best controller. By tuning the three parameters in the PID controller algorithm, the controller can provide control action designed for specific process requirements. The response of the controller can be described in terms of the responsiveness of the controller to an error, the degree to which the controller overshoots the set point and the degree of system oscillation. Note that the use of the PID algorithm for control does not guarantee optimal control of the system or system stability.Some applications may require using only one or two actions to provide the appropriate system control. This is achieved by setting the other parameters to zero. A PID controller will be called a PI, PD, P or I controller in the absence of the respective control actions. PI controllers are fairly common, since derivative action is sensitive to measurement noise, whereas the absence of an integral term may prevent the system from reaching its target value due to the control action.

IX. CONTROL LOOP BASICS

A familiar example of a control loop is the action taken when adjusting hot and cold faucets (valves) to maintain the water at a desired temperature. This typically involves the mixing of two process streams, the hot and cold water. The person touches the water to sense or measure its temperature. Based on this feedback they perform a control action to adjust the hot and cold water valves until the process temperature stabilizes at the desired value. The sensed water temperature is the process variable or process value (PV). The desired temperature is called the set point (SP). The input to the process (the water valve position) is called the manipulated variable (MV). The difference between the temperature measurement and the set point is the error (e) and quantifies whether the water is too hot or too cold and by how much. After measuring the temperature (PV), and then calculating the error, the controller decides when to change the tap position (MV) and by how much. When the controller first turns the valve on, it may turn the hot valve only slightly if warm water is desired, or it may open the valve all the way if very hot water is desired. This is an example of a simple proportional control. In the event that hot water does not arrive quickly, the controller may try to speed-up the process by opening up the hot water valve more-and-more as time goes by. This is an example of an integral control. Making a change that is too large when the error is small is equivalent to a high gain controller and will lead to overshoot. If the controller were to repeatedly make changes that were too large and repeatedly overshoot the target, the output would oscillate around the set point in a constant, growing, or decaying sinusoid. If the oscillations increase with time then the system is unstable, whereas if they decrease the system is stable. If the oscillations remain at a constant magnitude the system is marginally stable. In the interest of achieving a gradual convergence at the desired temperature (SP), the controller may wish to damp the anticipated future oscillations. So in order to compensate for this effect, the controller may elect to temper their adjustments. This can be thought of as a derivative control method.

If a controller starts from a stable state at zero error (PV = SP), then further changes by the controller will be in response to changes in other measured or unmeasured inputs to the process that impact on the process, and hence on the PV. Variables that impact on the process other than the MV are known as disturbances. Generally controllers are used to reject disturbances and/or implement set point changes. Changes in feed water temperature constitute a disturbance to the faucet temperature control process.In theory, a controller can be used to control any process which has a measurable output (PV), a known ideal value for that output (SP) and an input to the process (MV) that will affect the relevant PV. Controllers are used in industry to regulate temperature, pressure, flow rate, chemical composition, speed and practically every other variable for which a measurement exists.

9.1 PID CONTROLLER THEORY:

The PID control scheme is named after its three correcting terms, whose sum constitutes the manipulated variable (MV). The proportional, integral, and derivative terms are summed to calculate the output of the PID controller. Defining $u(t)$ as the controller output, the final form of the PID algorithm is:

$$u(t) = MV(t) = K_p e(t) + K_i \int_0^t e(\tau)\,d\tau + K_d \frac{d}{dt} e(t)$$

.....4.1

Where

K_p: Proportional gain, a tuning parameter

K_i : Integral gain, a tuning parameter

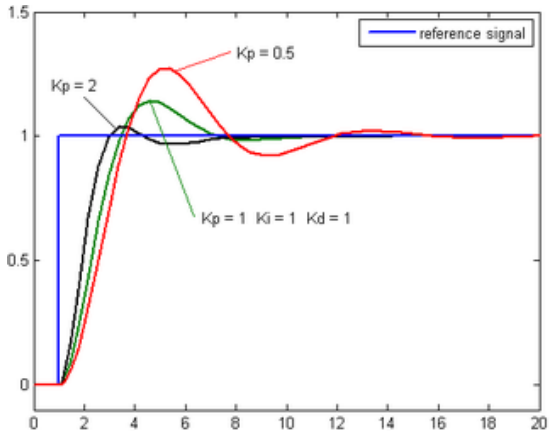
K_d: Derivative gain, a tuning parameter

e: Error = $SP - PV$

t : Time or instantaneous time (the present)

9.2 PROPORTIONAL TERM:

The proportional term makes a change to the output that is proportional to the current error value. The proportional response can be adjusted by multiplying the error by a constant Kp, called the proportional gain.



Plot of PV vs time, for three values of K_p (K_i and K_d held constant)

The proportional term is given by:

$$P_{out} = K_p e(t)$$

……(4.2)

A high proportional gain results in a large change in the output for a given change in the error. If the proportional gain is too high, the system can become unstable (see the section on loop tuning). In contrast, a small gain results in a small output response to a large input error, and a less responsive or less sensitive controller. If the proportional gain is too low, the control action may be too small when responding to system disturbances. Tuning theory and industrial practice indicate that the proportional term should contribute the bulk of the output change.

9.3 DROOP:

A pure proportional controller will not always settle at its target value, but may retain a steady-state error. Specifically, drift in the absence of control, such as cooling of a furnace towards room temperature, biases a pure proportional controller. If the drift is downwards, as in cooling, then the bias will be below the set point, hence the term "droop".

Droop is proportional to process gain and inversely proportional to proportional gain. Specifically the steady-state error is given by:

$$e=G/K_p$$

…….. (4.3)

Droop is an inherent defect of purely proportional control. Droop may be mitigated by adding a compensating bias term (setting the set point above the true desired value), or corrected by adding an integral term.

9.4 INTEGRAL TERM:

The contribution from the integral term is proportional to both the magnitude of the error and the duration of the error. The integral in a PID controller is the sum of the instantaneous error over time and gives the accumulated offset that should have been corrected previously. The accumulated error is then multiplied by the integral gain (Ki) and added to the controller output.

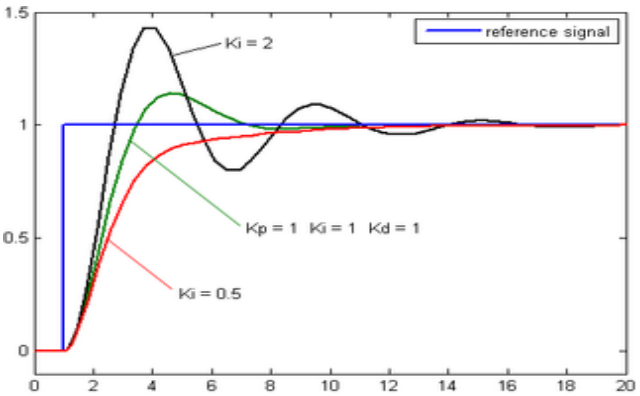


Fig 4.13 Plot of PV vs time, for three values of Ki (Kp and Kd held constant)

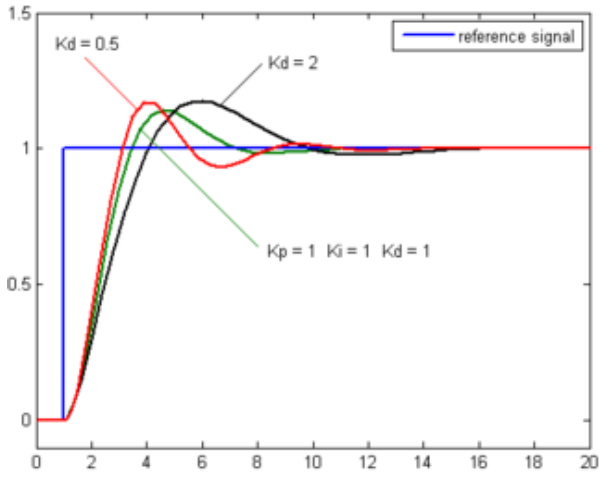
The integral term is given by:

$$I_{out} = K_i \int_0^t e(\tau)\, d\tau$$

The integral term accelerates the movement of the process towards set point and eliminates the residual steady-state error that occurs with a pure proportional controller. However, since the integral term responds to accumulated errors from the past, it can cause the present value to overshoot the set point value (see the section on loop tuning).

9.5 DERIVATIVE TERM:

The derivative of the process error is calculated by determining the slope of the error over time and multiplying this rate of change by the derivative gain Kd. The magnitude of the contribution of the derivative term to the overall control action is termed the derivative gain, Kd.



Plot of PV vs time, for three values of Kd (Kp and Ki held constant)

The derivative term is given by:

$$D_{out} = K_d \frac{d}{dt} e(t)$$

(4.5)

The derivative term slows the rate of change of the controller output. Derivative control is used to reduce the magnitude of the overshoot produced by the integral component and improve the combined controller-process stability. However, the derivative term slows the transient response of the controller. Also, differentiation of a signal amplifies noise and thus this term in the controller is highly sensitive to noise in the error term, and can cause a process to become unstable if the noise and the derivative gain are sufficiently large. Hence an approximation to a differentiator with a limited bandwidth is more commonly used. Such a circuit is known as a phase-lead compensator.

9.6 PROPOSED CONTROL STRATEGY:

Both open loop and closed loop control for the proposed integrated converter is analysed. PID controller is used for the closed loop control of buck-integrated SEPIC converter. In the case of open loop control, the pulses are generated by the following equation:

$$V_o = V_{dc} d_c + \frac{V_{pv} d_p}{(1 - d_p)}$$

Where:

$V_{o\ is}$ the output voltage (V).

$V_{dc\ is}$ the DC source voltage (V).

$V_{pv\ is}$ the PV voltage (V).

d_c is the duty cycle of Buck converter.

$d_p$is the duty cycle of SEPIC converter.

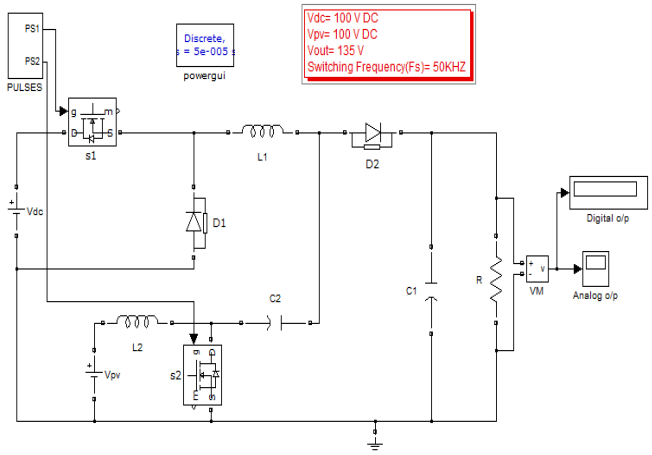
X. SIMULATION AND RESULT

Simulation has become a very powerful tool on the industry application as well as in academics, nowadays. It is now essential for an electrical engineer to understand the concept of simulation and learn its use in various applications. Simulation is one of the best ways to study the system or circuit behaviour without damaging it. The tools for doing the simulation in various fields are available in the market for engineering professionals. Many industries are spending a considerable amount time and money in doing simulation before manufacturing their product. In most of the research and development work , the simulation plays a very important role. Without simulation it is quite impossible to proceed further. It should be noted that in power electronics , computer simulation and a proof of concept hardware prototype in the laboratory are complimentary to each other. However computer simulation must not be considered as a substitute for hardware prototype.

10.1 SIMULATION BLOCK DIAGRAM AND RESULT FOR OPEN LOOP CONTROL

Here, a 100V input voltage is given to Buck converter. Another 100V input voltage which represents the output voltage of PV module is given to the SEPIC converter. An output of 135.1V is obtained. The pulse for

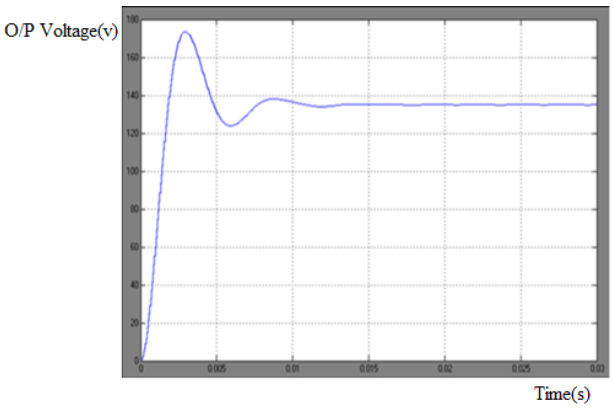
the switch in Buck and SEPIC converter is developed by the following equation.



Simulink model for open loop control of Buck-integrated SEPIC converter

$$V_o = V_{dc} d_c + \frac{V_{pv} d_p}{(1 - d_p)} \qquad (5.1)$$

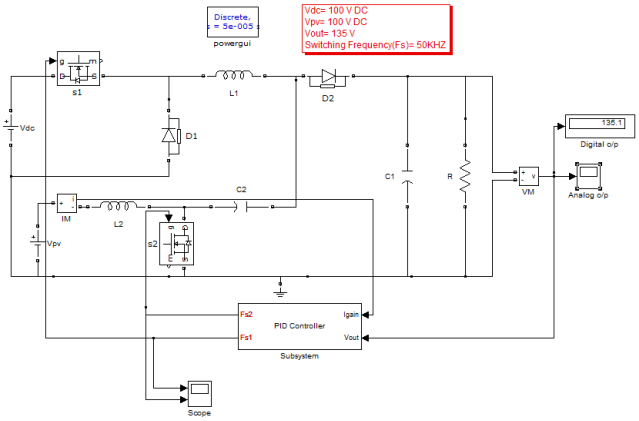
10.2 Simulation Result:



Simulation result for open loop control of Buck-integrated SEPIC converter

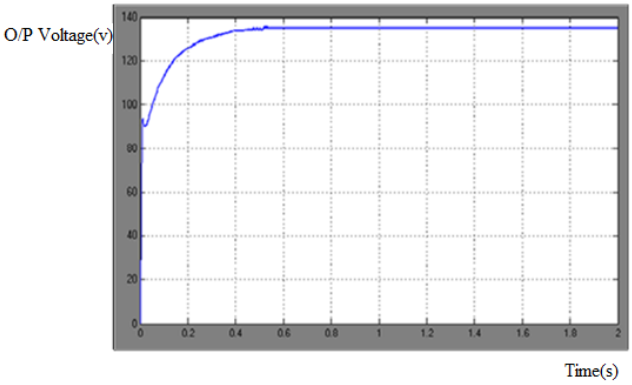
10.3 Simulation Block Diagram and Result For Closed Loop Control

Here also 100V input supply is given to Buck and SEPIC converter. An output of 135v is obtained. The pulse for the switch in Buck and SEPIC converter is developed by PID controller. Reference voltage in the PID controller is set as 135V.



Simulink model for closed loop control of Buck-integrated SEPIC converter

Simulation Result:



Simulation result for closed loop control of Buck-integrated SEPIC converter

10.4 RESULTS AND DISCUSSION

It was observed that the percentage differences in optimal-THD performance between the equal and unequal source cases generally increase with the number of waveform levels. The magnitudes of the waveform harmonics (up to the 49th) are presented in Table for the 5-, 7-, 9-, 11-, and 13- level output voltage waveform cases corresponding to the theoretical THD-optimal solutions. Note that for the 13-level case, the most significant harmonics are at frequencies above the 25th one, so they are of lesser concern. In Fig. 6, the magnitudes of the lowest harmonics for the various 9-level optimal waveforms are compared. These clearly show the relatively significant content in the lowest harmonics for the optimal THD and THD with HE cases.

XI. CONSIDERATION OF DEVICE VOLTAGE DROPS

For Highly Resistive Loads

To account for the non-zero voltage drops of IGBTs and diodes in the output waveform produced by the cascaded H-bridges, the following calculations were carried out to generate more accurate step levels in the output voltage for

highly resistive loads. The exact voltage drops of active switches depend on device current direction and magnitude but by using the typical value of voltage drop for these switches at nominal current it is possible to obtain better approximations of the desired voltage levels. Here VSWand VDare used to denote typical values of the voltage drop for each IGBT and each diode, respectively. In this study, the calculations were performed for conditions where the output voltage and current of each cell have directions signifying power delivery; this is always valid for resistive and highly resistive loads. The total voltage drop across the switches for a cell when it is generating a non-zero voltage is 2VSWand if the cell's output voltage is zero then the voltage drop is VSW+ VD. Hence, the ith voltage level can be calculated as

$$L_i=\sum_{j=1\ldots i}^{n}\{E_j'\} - i(2V_{SW}) + \{s-i\}V_{SW} + VD \quad (5.2)$$

Where is the actual dc voltage of each jth H-bridge cell and s is the number of steps in the waveform. Equation (5.2) can be simplified to

$$L_i=\sum_{j=1\ldots i}^{n}\{E_j'\} - \{s+i\}V_{SW} + \{s-i\}V_D \quad (5.3)$$

For igreater than one, the ith voltage step (i.e. Ei) is

$$E_i=Li-Li_{-1}=E_1'-(V_{sw}-V_d)=E_1'-(V_{sw}+V_d) \quad (5.4)$$

And the first step voltage is equal to the first level so

$$E_1=L_1=E_1'-[S+1(V_{SW}+(S-1)V_d) \quad (5.5)$$

Based on the definition of the voltage ratio of the waveform step, the following relation can be expressed. Using (5.5) and by considering the voltage ratio between each step for igreater than one, the actual dc voltage source needed to generate Eiin the output waveform was calculated from

$$E_1'=\rho_1 E_S(V_{SW}-)V_d) \quad (5.6)$$

and the voltage source of the first H-bridge cell can be calculated as

$$E_1'=\rho_1 E_S+[S+1(V_{SW}+(S-1)V_d)$$

By using the above, it was possible to choose the voltage source values that generated the required voltage steps in the output waveform more accurately for highly resistive loads. Note that using the adjusted dc voltage source values Ei' will compensate for the effect of switch and diode voltage drops when the load's current is leading and lagging the output voltage of the converter by a maximum of θ_1. In this case, no change in current direction occurs when applying voltage levels other than zero level to the load; therefore the phase difference between the output voltage and current does not matter when it is less than θ_1. However, if the load's power factor angle is greater than θ_1, this results in a small step in the output waveform at the point when the output current changes its direction. If the magnitudes of the device voltage drops are small compared to the voltage levels of the output waveform, then their impact on waveform distortion will be correspondingly small. Otherwise, the effect of diode and IGBT voltage drops on the converter's output voltage depends on the amplitude of the output current and the load's power factor.

FOR MODERATELY LAGGING POWER FACTOR LOADS

Accounting for the device voltage drops when the load has a moderate lagging power factor (e.g., 0.8, although what is meant by this is that the distorted load current crosses zero with positive slope at an angle of cos-1(0.8)) yields a half wave symmetric waveform (Fig 5.5) for v0(t). Hence, considering the 5-level case with load current crossing zero at ϕ1, the Fourier series expansion of vo(t) is no longer given by (1), (2), but by

$$vo(t) = \sum_{odd}\{ V_{ha}\cos(h\omega t) + V_{hb}\sin(h\omega t) \} \quad (5.8)$$

with

$$V_{ha}=\frac{4}{h\pi}\ [2V_{SWD}\sin(h\ \phi_1)] \quad (5.9)$$

$$V_{hb}=\frac{4}{h\pi}[E_1\cos(h\theta_1)+E2\cos(h\theta_2)+2V_{SWD}\{\cos(h\theta 1) - \cos(h\ \pi\phi_1\}] \quad (5.10)$$

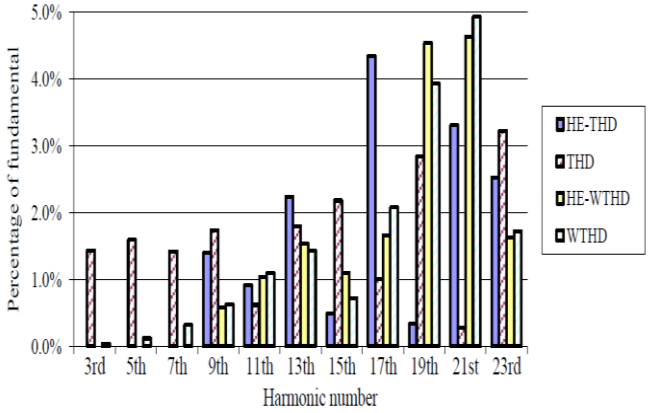
where$V_{SWD}= V_{SW}+ V_D$.

Then the harmonic components have magnitudes given by $V_h= \sqrt{\sqrt{v_{ha}^2} + \sqrt{v_{hb}^2}}$ (5.11)

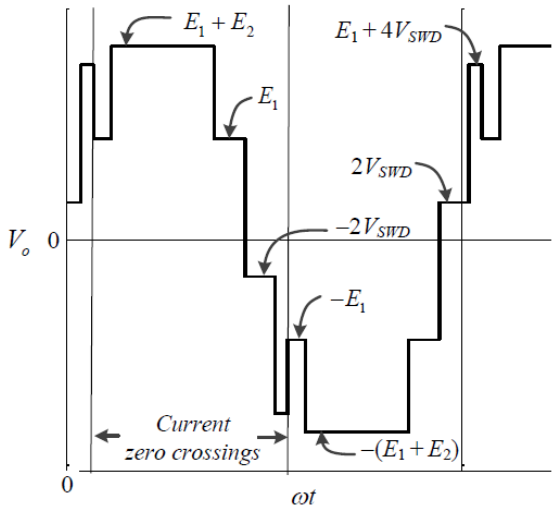
.

It was then found that imposing the HE requirement meant large changes in ρ1, $\theta 1$, $\theta 2$, to achieve optimal THD even for small VSWD, e.g., for 1%VSWD(%VSWDbeing defined as VSWD/E2 x 100%), (ρ1, $\theta 1$, $\theta 2$,) = (3.07, 24.2°, 52.8°) are needed to achieve 20.8% THD, while for 2%VSWD, (ρ1, $\theta 1$, $\theta 2$) = (5.45, 26.7°, 54.6°) are needed to achieve 24.1% THD. This is significantly different than the non-HE case, where for up to about 30%VSWD only minor adjustments of the ρ1, $\theta 1$,2, can achieve optimal THD as

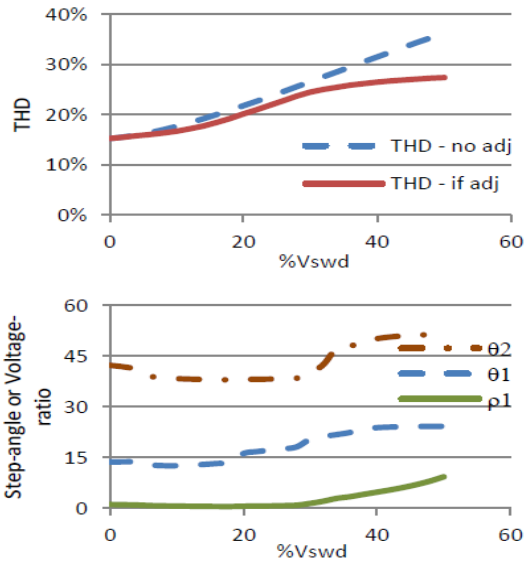
can be seen . On the other hand, up to about 30%VSWD, not adjusting the ρ1, θ1 ,2, from their nominal values to account for the device drops will only increase THD by no more than 2% over the achievable minimum. For example, at 20%VSWD, using the settings for 1.0 pf load of (ρ1, θ1 , θ2,) = (1.09, 13.7°, 42.2°) yields 21.75% THD, up from 15.25%; while adjusting for the device voltage drops with a 0.8 pf load using (ρ1, θ1 , θ2,) = (0.58, 16.1°, 38.1°) yields 20.13% THD.



Comparison of the percentage magnitudes of the lowest harmonics (9-level waveforms).



Inverter output voltage (5-level) waveform considering device voltage drops for a moderately-lagging power factor load.



Analytical THD vs %VSWDbefore, and after, adjusting (ρ1, θ1θ2); and (ρ1, θ1θ2) values vs %VSWDfor optimal THD.

EXPERIMENTAL VERIFICATION

In order to verify the analysis, a hardware prototype of the inverter was tested. Each dc source was implemented by a Sorensen DHP 400-25 dc power supply connected in parallel with a United Chemi- Con 3.9mF 450V electrolytic capacitor. In practice, the dc sources can be derived from a native ac source such as the utility grid via transformer rectifier units, or from a native dc source such as photovoltaic panels. In either case, regulation of the dc inputs to the multilevel inverter is required to maintain the proper voltage ratios for minimal distortion. This can be achieved by the use of controlled rectifiers or regulated dc-dc converters, respectively, with the switch control signals being computed and generated by a central supervisory controller, such as a programmable digital circuit board, in response to source and/or load changes.

For all tests, the last H-bridge cell output was a 100 V step with the other cells outputting appropriate voltage levels relative to this. To generate the switching angles, a CY37128P84 complex programmable logic device was used. Its clock frequency of 1 MHz, which yields angles with 0.02° accuracy for a 60 Hz output waveform, was sufficiently accurate for this study. Fibber optic cables were used to send these switching signals to the CM75DU-24F IGBTs. Tests were carried out to produce 5-, 7-, and 9-level waveforms.

RESULTS FOR RESISTIVE LOAD

Tests were carried out to produce 5-, 7-, and 9-level waveforms. For all tests, the last H-bridge cell output was a 100 V step with the other cells outputting appropriate

voltage levels relative to this. The VSW and VD were 1.2 V and 0.8 V, respectively.

THE 9-LEVEL WAVEFORM

Fig. 5.9 shows the output waveform of the 9-level inverter to achieve minimum THD using unequal sources. This test, which used appropriate adjusted source values Ei', yielded a THD of 7.58% with m1 = 3.35, which are very close to the theoretical values. And Table 5.3 shows that a very good match was obtained between the theoretical and experimental harmonic magnitudes for this optimal THD case. Experimental values of THD, WTHD and m1 corresponding to the various THD and WTHD cases for unequal 9-level waveforms are given in Tables 5.1 and 5.2.

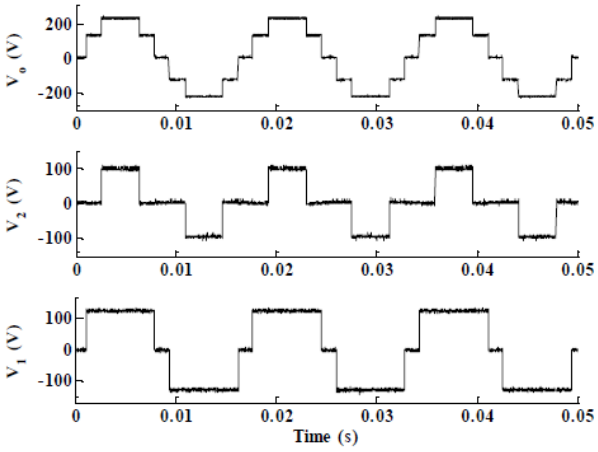
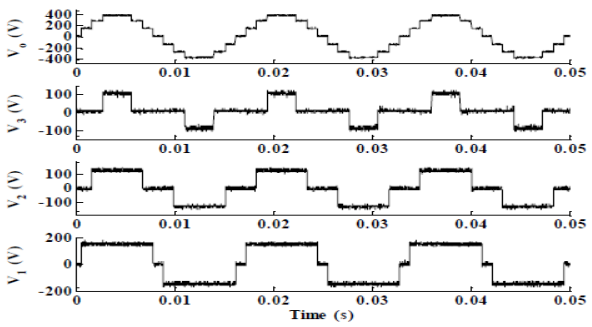


Fig. 5.8 Output voltage (5-level) of the inverter and output voltage of each H-bridge to achieve optimal THD with HE.

RESULTS FOR 0.8 LAGGING POWER FACTOR LOAD

Tests were carried out to produce 5-level optimal THD waveforms. For all tests, the load was set at R = 4.1 Ω and L = 12.6 mH, and the second H-bridge cell output was a 10 V step with the other cell outputting appropriate voltage levels relative to this. The voltage drops for the IGBTs were found to be 1.45 V and for the diodes to be 0.6 V, which yielded about 20%VSWD. Using the settings for resistive loads of (ρ1, θ1, θ2) = (1.09, 13.7°, 42.2°), so E1' = 15.85 V and E2' = 10.85 V, resulted in 21.12% THD, up from 15.45% (measured). Adjusting for the device voltage drops for a 0.8 lagging power factor load using (ρ1, θ1, θ2) = (0.58, 16.1°, 38.1°), with E1' = 10.75 V and E2' = 10.85 V, yielded 19.73% THD; the obtained waveforms are shown in Figure. These differ only slightly from the analytical values.



Output voltage (7-level) of the inverter and output voltage of each H-bridge to achieve optimal WTHD.

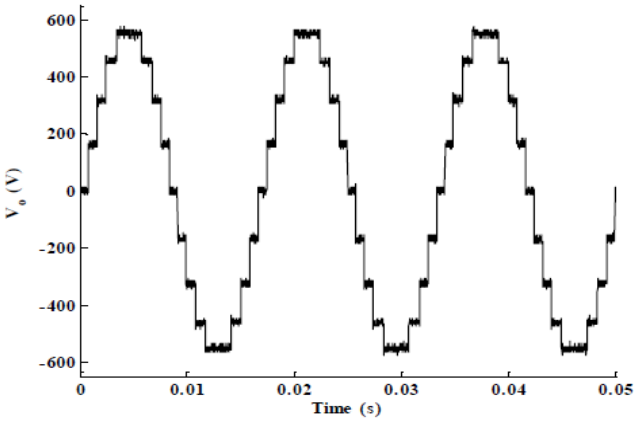


Fig.5.10. Output voltage (9-level) of the inverter for optimal THD.

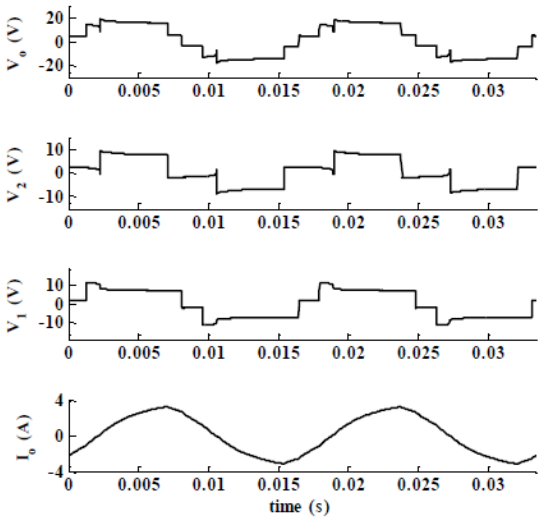


Fig. 13. Output voltage (5-level) of the inverter for optimal THD with a 0.8 lagging pf load and 20%V_{SWD}.

Fig 5.11 output voltage (5-level)of inverter for optimal THD with a 0.8 Lagging pf load and 20%Vsw

Waveform levels	Case	ρ_1	ρ_2	ρ_3	ρ_4	ρ_5	ρ_6	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	m_1	%THD	Expt m_1	Expt %THD
5	HE	1.05	1					14.5°	46.4°					1.70	15.79	1.70	15.68
5	No HE	1.09	1					13.7°	42.2°					1.80	15.25	1.79	15.17
*5	No HE	0.58	1					16.1°	38.1°					1.43	20.13	1.39	19.73
7	HE	1.18	1.11	1				9.95°	30.7°	56.6°				2.67	10.64	2.65	10.61
7	No HE	1.29	1.15	1				10.2°	30.8°	52.5°				2.86	10.27	2.84	10.19
9	HE	1.18	1.43	1.29	1			7.26°	21.9°	40.9°	62.9°			3.93	7.97	3.92	7.84
9	No HE	1.03	0.99	1.04	1			6.91°	20.8°	35.5°	55.9°			3.35	7.62	3.35	7.58
11	HE	1.54	1.42	1.30	1.20	1		6.70°	20.2°	33.7°	47.6°	66.7°		5.15	6.02		
11	No HE	1.67	1.58	1.39	1.15	1		6.88°	20.6°	34.4°	48.2°	63.0°		5.50	5.86		
13	HE	1.77	1.78	1.80	1.64	1.25	1	5.76°	16.4°	28.5°	41.7°	54.7°	70.4°	7.34	5.00		
13	No HE	1.56	1.56	1.51	1.50	1.25	1	4.85°	16.1°	26.5°	38.8°	52.1°	66.2°	6.74	4.84		

Table 5.1 Minimum Achievable the Results for Unequal Dc Sources (Up To 49th Harmonic) {* - 0.8 Lagging Pf Load, 20%*Vswd*}

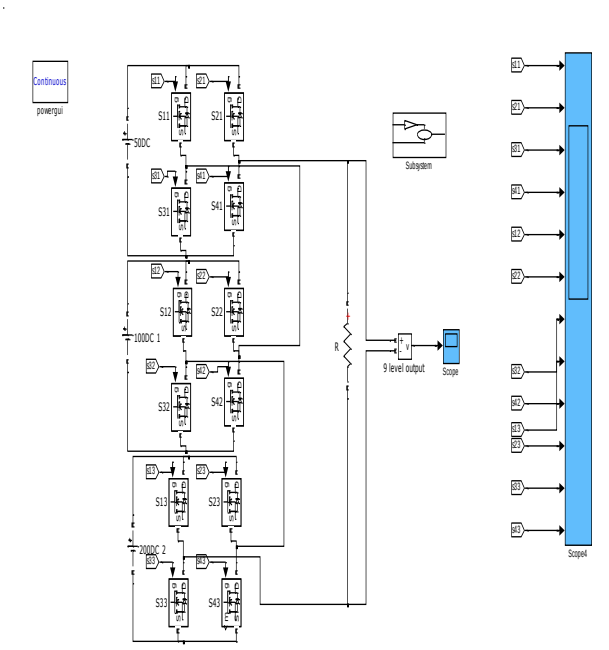
Waveform levels	Case	ρ_1	ρ_2	ρ_3	ρ_4	θ_1	θ_2	θ_3	θ_4	m_1	%WTHD	Expt m_1	Expt %WTHD
5	HE	1.26	1			15.8°	49.5°			1.86	1.42	1.85	1.43
5	No HE	1.28	1			15.7°	49.3°			1.88	1.41	1.87	1.42
7	HE	1.48	1.34	1		10.8°	33.5°	59.2°		3.08	0.68	3.06	0.68
7	No HE	1.47	1.34	1		10.9°	33.4°	58.7°		3.09	0.68	3.06	0.68
9	HE	1.66	1.59	1.36	1	8.47°	25.6°	43.7°	64.8°	4.48	0.40	4.44	0.41
9	No HE	1.66	1.57	1.37	1	8.37°	25.4°	43.5°	64.1°	4.49	0.40	4.45	0.40

Table 5.2 Minimum achievable WTHD results for unequal dc sources (up to 49th harmonic)

Waveform levels	Harmonic magnitudes as a percentage of the fundamental's magnitude (%)																					
	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31	33	35	37	39	41	43	45	47	49
Theory 5	4.1	5.11	2.51	2.05	6.12	8.88	3.38	1.16	.12	1.65	1.15	4.36	3.21	.05	.37	1.06	.34	2.22	2.81	.84	.36	.50	.82	.86
*5	12.5	5.99	5.33	2.16	5.04	7.55	4.35	2.29	4.47	3.08	1.32	1.35	2.35	.56	2.62	3.61	1.75	.84	.55	.68	.55	2.11	2.44	.51
7	1.51	2.49	2.32	1.12	.67	2.11	2.42	6.95	3.48	.36	.33	.25	.82	.54	.76	2.27	3.21	.90	.01	.42	.34	.35	.81	.06
9	1.43	1.59	1.42	1.73	.62	1.80	2.18	1.01	2.84	.28	3.22	2.66	2.35	1.75	.79	.73	1.20	.16	1.15	.10	.61	.04	.19	.79
11	.40	.77	.98	.93	.70	.22	.23	.67	.73	.37	.22	3.98	3.68	.32	.02	.02	.12	.29	.21	.05	.30	.45	.25	.19
13	.30	.38	.57	.67	.62	.34	.43	.45	.01	.97	.93	.62	2.31	.17	2.52	2.11	1.61	.65	.19	.16	.28	.24	.30	.38
Experiment 5	4.4	4.95	2.48	2.00	6.11	8.87	3.45	1.07	.13	1.62	1.11	4.26	3.17	.12	.33	1.02	.34	2.08	2.67	.84	.29	.48	.76	.74
*5	10.6	7.70	4.72	1.09	4.22	7.97	5.18	1.79	5.10	3.26	.73	.91	2.34	1.03	2.39	3.93	2.03	.62	.84	.38	.24	1.92	2.58	.78
7	1.56	2.37	2.47	1.13	.77	2.11	2.35	6.91	3.50	.33	.37	.29	.82	.49	.77	2.13	3.09	.89	.03	.43	.29	.34	.73	.02
9	1.54	1.43	1.64	1.63	.68	1.94	2.32	1.12	2.75	.30	3.15	2.60	2.30	1.77	.71	.69	1.19	.20	1.10	.06	.53	.01	.20	.66

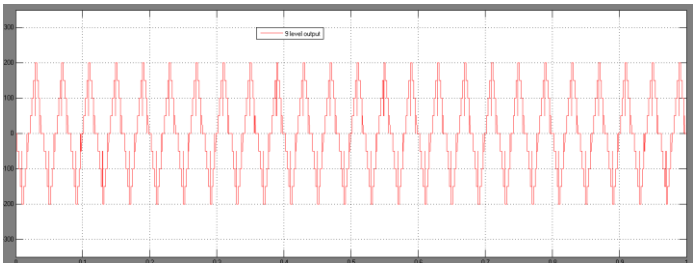
Table 5.3 Harmonic magnitudes of the THD-optimal waveforms {* - 0.8 lagging PF load, 20%v_{swd}}

SIMULINK MODEL FOR THE PROPOSED SYSTEM



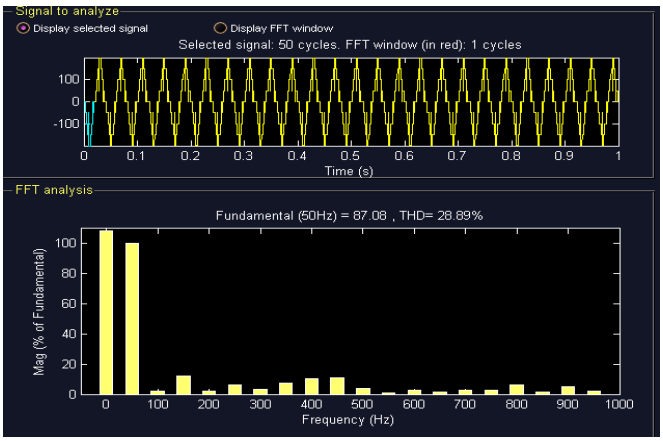
Simulink Model forthe Proposed System

SIMULATION OUTPUT FOR THE PROPOSED SYSTEM（9 LEVEL OUTPUT）



Simulation Output For The Proposed System（9 Level Output）

SIMULATION OUTPUT USING FOURIER ANALYSIS



Simulation Output Using Fourier Analysis

UTILISED CONVERTER PARAMETERS

Components	Parameter
Input DC source voltage	100V
Input PV module voltage	100V
Output Voltage	135V
Switching frequency	50 KHz
Inductors	L_1 = 700µH, L_2 = 700µH
Capacitors	C_1 = 16000µF, C_2 = 150µF
Resistor	2.5Ω

XII. CONCLUSION

This paper has taken the problem of determining the minimum achievable Total harmonics and without harmonics reduction of the staircase-modulated output voltage of single-phase multilevel inverters. The THD values together with step angles and dc source ratios obtained for the 9-level (4-step) & 5-, 7- and 9-level output voltage waveform cases. The results show that the use of unequal dc source voltages achieves lower minimal THD and WTHD than if equal source voltages were used, as expected. Mainly this paper used for hybrid system like hybrid vehicles and hybrid power plant. For instance, a voltage THD of less than 5% can be achieved by an output voltage waveform with 13 unequal levels but not with 13 equal levels.

Moreover, the results also indicate that requiring the elimination of the lowest harmonics yields slightly inferior THD than if this requirement was not imposed. These are smaller than that obtained by optimizing with respect to THD. Finally, the results suggest that when the load has a moderate lagging power factor, attempting to maintain selective HE to reduce a multilevel inverter's output voltage distortion is actually counter-productive. Whereas using the (ρ1, θ1 , θ2) values, in the 5-level case, corresponding to THD without HE for unity power factor loads yields THD that's not much more than the achievable minimum for up to about 30%VSWDor, equivalently, as the output's modulation index is decreased by up to about 30%.

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