

A Review on Different Operational Transconductance Amplifier Design Using CMOS Technology

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ABSTRACT

The operational transconductance amplifier is a widely used analog processing block. In recent years, the development of OTA with very low conductivity, low power, low voltage and improved linearity has been used in various applications. In this paper mainly discussed the various design architecture of operational transconductance amplifier using CMOS technology in different fields.

Keywords: - CMOS, Operational Transconductance Amplifier, RF Communication, High Frequency.

I. INTRODUCTION

In portable high performance, high density ICs the power consumption should be considerably minimized [1-2]. This, in turn shrinks down IC both in terms of area and power supply. Hence ICs are required to be designed in deep submicron technology with low voltage and power supply. OTA are widely use in wireless analog processing applications such as continuous time OTA-C filters, four quadrant multiplier, mixer, modulator ,data converter, variable gain amplifier, oscillators and other interface circuits. In many of these applications OTA at the input stage determines the overall linearity of the system [3]. So, it is required to improve the linearity of OTAs. As device sizes, supply voltage and power consumption are scaled down to achieve higher operating speeds, obtaining high linearity with reasonable output signal levels becomes ever challenging.

II. DIFFERENT OPERATIONAL TRANSCONDUCTANCE AMPLIFIER DESIGNING TECHNIQUES

A. Floating Gate Low Power OTA

In [4], a low voltage class-AB OTA Fig 1 using the quasi floating gate MOSFET (QFG-MOS) is proposed. It is known that QFG-MOS is suitable for low voltage operation [5]. The circuit uses positive feedback to enhance the input impedance, and novel feed-forward technique to simultaneously suppress common-mode signals and enhance the differential-mode signals. The circuit exhibits large input/output swing with good linearity.

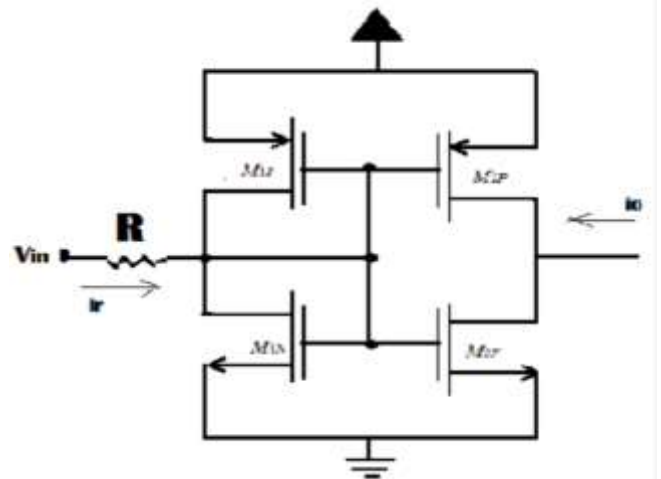


Fig. 1. Single ended class AB linear OTA

The differential OTA in Fig. 2 is known as Pseudo differential amplifier (PDA). One can see that the differential mode transconductance (G_{dm}) is the same as the common mode transconductance (G_{cm}), making the OTA prone to interferences and supply noises. To suppress the common mode response, a newly developed feed-forward circuitry has been proposed. The technique employs feed-forward amplifier (FFA) and body-driven as shown in Fig. 2. As seen, FFA consists of two independent CMOS inverters ($M2AN,P$ and $M2BN,P$) and inverting amplifiers ($-A$), which serves two purposes: 1) to suppress the common-mode current signals (i_{o1} and i_{o2}), and 2) to enhance the differential transconductance (G_{dm}) of the system.

From Fig. 2, the differential-mode (G_{dm}) and common mode (G_{cm}) transconductance gains can be derived and shown as

$$G_{dm} = g_{m2N,P} + A g_{mb2N,P}$$

$$G_{cm} = g_{m2N,P} - A g_{mb2N,P} \quad (1)$$

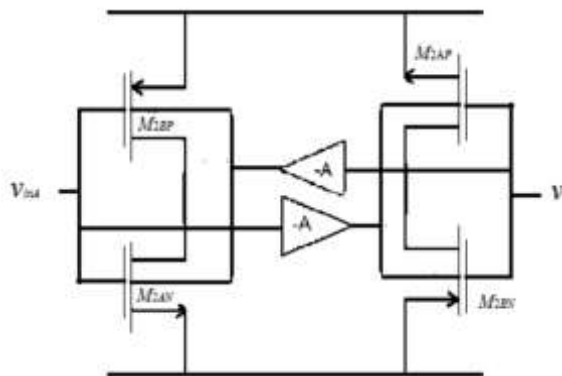


Fig. 2. Class-AB linear OTA

Where A is the voltage gain of the inverting amplifier, $g_{m2N,P}$ and $g_{mb2N,P}$ are the gate and the body transconductance of $M2AN, P$ ($M2BN, P$), respectively. The proposed QFG-inverter is employed, enabling the circuit to operate under low voltage supply. Feed-forward technique is used to suppress the common-mode response. The circuit demonstrates wide input/output swing and good linearity over an entire range of the input signal. The differential-mode gain is increased, while the common-mode gain is suppressed.

B. Pseudo Differential OTA

Many approaches have been proposed to design low voltage OTA using pseudo-differential (PD) configurations. PD is based on two independent inverters without tail current source. It is known that avoiding the voltage drop across the tail current source, in a PD structure, allows wider input and output ranges, and makes the architecture attractive for low power supply applications. However, PD structure requires an extra common-mode feedback (CMFB) circuit, which serves two purposes: 1) to fix the common-mode voltage at high impedance nodes and 2) to suppress the common-mode signal components. As shown in fig.4 the pseudo differential amplifier has an internal input common mode detector ($M1, M2$) and a feed forward path $M4$ to remove DC component of the output current. The node named V_{cm} contains common mode information of the input signal. Since this G_m cell is usually used in a chain structure i.e. in G_m -C filter its common mode extracting feature can help the previous blocks to have a better estimation of their output common voltage [6].

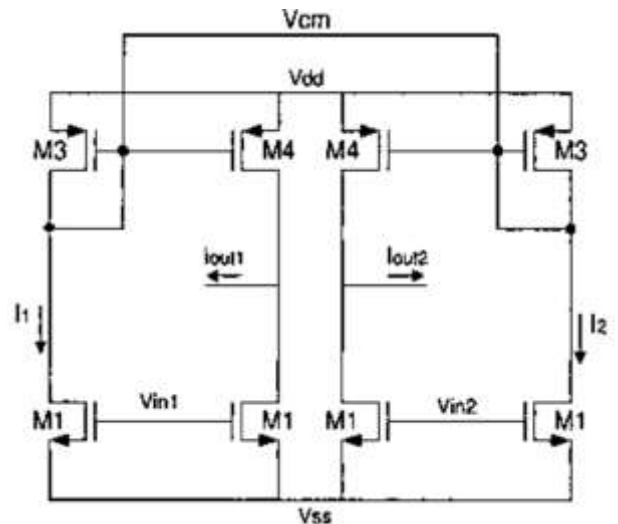


Fig. 3. Basic pseudo differential amplifier structure

C. OTA Design Using Multi tanh Linearization Technique

In multi-tanh linearization technique multiple pair of differential input are used that W/L ratio of each pair is $1/4$. In multi-tanh technique used for the low power CMOS circuit design for low frequency applications. In this technique differential input is taken by the input pair of the MOS and single ended output is taken [7].

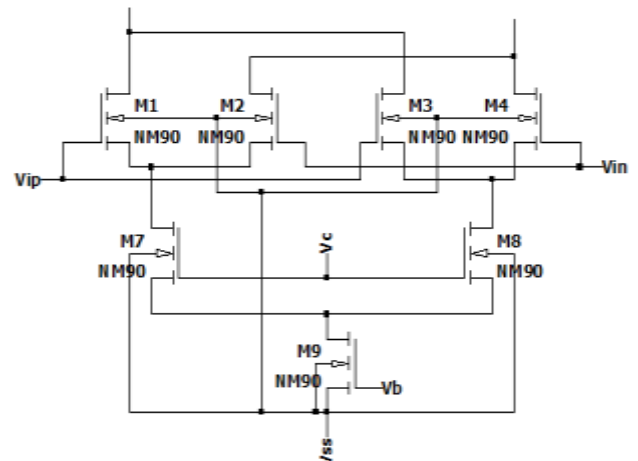


Fig. 4. OTA Design Using Multi tanh Linearization Technique

D. Two stage Bulk driven OTA

Raha [8], introduced the previous technology, expands the digital circuit to operate at low voltage and reduces energy consumption. All physical signals are analog in nature, so we need an analog interface module, like the front end. In the proposed design implementation, the mass-driven operational transconductance amplifier with local common mode feedback, which shows OTA design to realize LPF filter with very low power consumption and low frequency. In order to further reduce the cut off frequency, a capacitance multiplier is used.

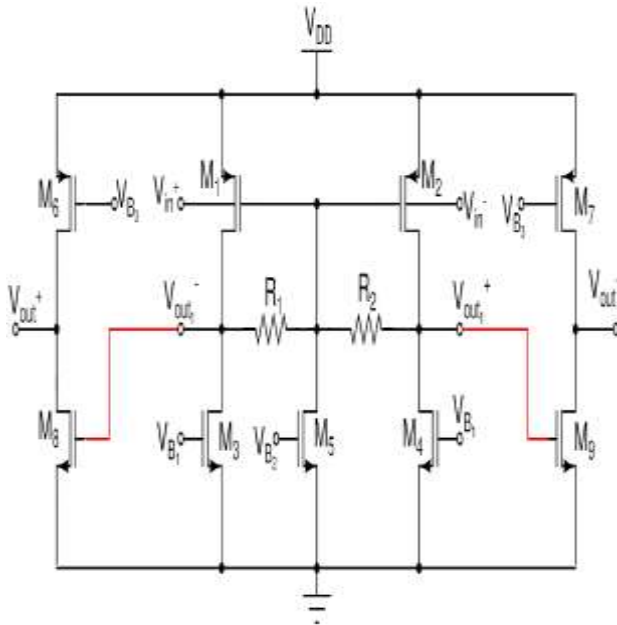


Fig. 4. OTA Design Using Multi tanh Linearization Technique

E. Source Degeneration OTA

Edwin explained that the demand for medical surveillance products is growing worldwide. Low-power and low-voltage attributes are important issues that need to be addressed in the circuit. It is used for personal health monitoring and prolongs battery life. In this, Edwin introduced a biomedical amplifier designed to detect electrocardiogram signals. The design includes a high pass filter, a calculation filter. It consists of a resistance amplifier (OTA), two linear amplifiers with variable gain, three low-pass filters (LPF) and an operational transistor amplifier (ORA). In particular, VGA and LPF use log compression technology.

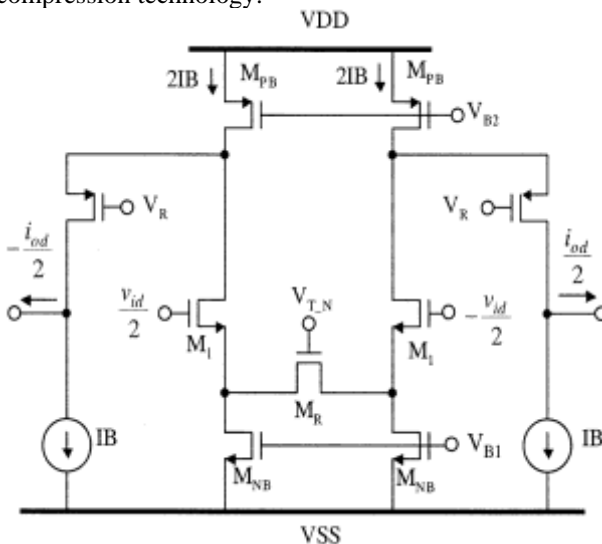


Fig. 5. Source Degeneration OTA Structure

F. Cross-Coupled Differential Input OTA

The circuit topology utilizes a cross-coupled differential input pair and a current mirror-based architecture with differential active loading and a high gm. The transconductance value of around 750 μ S was measured at the 0V differential input. Also, the pseudo differential OTA was designed and simulated on the same 65 nm CMOS technology node, to have a better circuit performance comparison. In the succeeding analysis, the MOSFETs are assumed to be operating in saturation [10, 11].

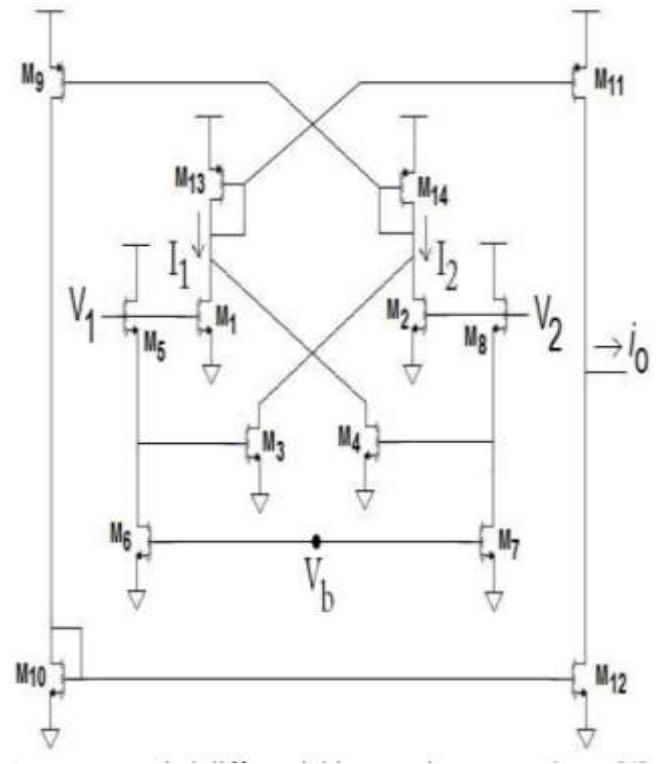


Fig. 6. Cross-coupled differential input pair transconductor

G. Folded Cascode OTA

Here as shown in Fig. 7, the schematic diagram of Folded Cascode OTA. In this type OTA, in the first stage. In the first stage of folded Cascode OTA, there are four transistors at the output side to have high output resistance. All the transistors are working in the saturation region ($V_{ds(sat)} \geq 0.1V$). A differential NMOS pair s are used as input. And in the second stage of OTA is in cascade with the first stage and its used to achieve higher gains while boosting the output swing voltage [12].

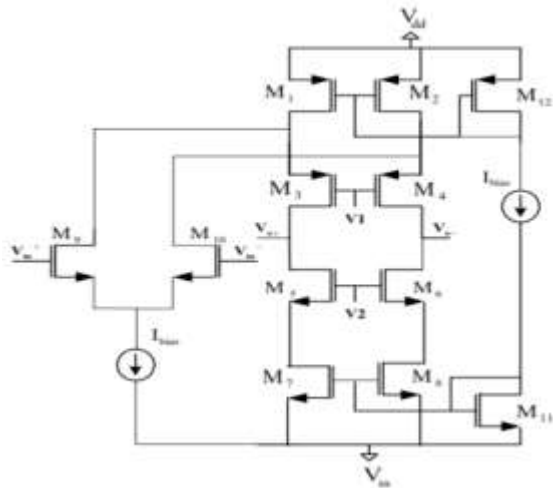


Fig. 7. Folded Cascode OTA

III. CONCLUSIONS

In this paper various topologies of operational transconductance amplifier (OTA) are studied and discussed for RF communication and different application. The operational transconductance amplifier (OTA) design approach is based on using CMOS advanced process technologies with proper topology to optimize the performance parameters of OTA.

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