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Implementing a Full Adder/ Full Subtractor Using Parity Conserving Reversible Gates

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ABSTRACT

The generally utilizing CMOS innovation executing with irreversible logic will hit a scaling limit past 2020 and the significant constraining element is expanded power dispersal. The irreversible logic is supplanted by reversible logic to diminish the power scattering. The gadgets executed with reversible logic doors will have interest for the forthcoming future computing advances as they expends less power. Reversible logic has applications in Low Power VLSI, Quantum Computing, Nanotechnology and Optical computing. This paper proposes the outline of an ideal fault tolerant Full adder/Full subtractor. For this logic circuit input equality and yield equality is same henceforth it is called equality saving circuit. The proposed technique require less intricacy, less equipment, least number of entryways, least number of trash sources of info and least number of steady contributions than existing strategies. List Terms—Reversible Logic, Quantum computing, Fault Tolerant, Full Adder, Full Subtractor.

Keywords:- VLSI, Reversible

I. INTRODUCTION

In the course of the most recent couple of years, reversible logic has been broadly utilized as a part of various advances, for example, DNA computing, Bio-informatics, Quantum computing and Nanotechnology. In reversible logic bit misfortune is recouped by special info yield mapping where in customary logic it isn't conceivable. It is one of particular component of reversible logic. In reversible logic the info pattern is recuperated from its yield pattern yet it fizzles traditional logic. In 1961, the exploration of R. Landauer showed that the measure of vitality dispersed for each data bit misfortune is at any rate kTln2 joules, where k is Boltzmann consistent and T is temperature at which framework task is performed [1]. The measure of vitality which is dispersed because of one piece data misfortune is little. However, in fast computational works the quantity of data bits is more. At that point the warmth dispersal is likewise more. This dispersal influences the execution and diminishes the lifetime of framework. In 1973, Bennet showed that kTln2 vitality won't be dispersed if the data sources can recuperate from its yield [2]. Henceforth the power scattering will be zero if a system contains just reversible logic doors. The enhancement parameters for the blend of reversible logic circuit are 1. Least number of doors 2. Least quantum cost 3. Least number of steady data sources 4. Least number of refuse yields 5. Least defer Also coordinate fan-out isn't permitted in the blend of reversible logic doors since one-to-numerous idea isn't reversible. By utilizing extra reversible logic doors the fanout can be accomplished. The combination of reversible logic is unique in relation to the customary logic [3]. To start with, the reversible circuit ought not have fan-out i.e., the yield of any door is associated as contribution to any entryway once as it were. Furthermore, the info yield patterns have coordinated correspondence. In conclusion, the circuit must be non-cyclic. Notwithstanding these a circuit is called reversible if the yields are connected at the yield at that point inputs are imitated at the information i.e., we are duplicating the contributions from yields. The fault tolerant reversible entryways are exceptional doors in reversible entryways. the fault tolerant doors fulfills the property of equality protecting i.e., the equality of information and yield is same. A logic piece is called equality safeguarding if each door in that is equality protecting [4]. On the off chance that a logic piece is executed with fault tolerant entryways then those doors won't require additional hardware to check blunders which happen in calculation or correspondence. Expansion is one of the basic task in increase and division calculations. It assumes an imperative part in numerous applications like DSP processors, Micro processors

and in computing gadgets. Henceforth, it is required to configuration quick adder. This paper introduces a novel outline of reversible improved fault tolerant Full adder/Full subtractor. This paper proposes a proficient way to deal with actualize 1-bit adder which will assume an imperative part in future quantum computers.

II. EXISTING METHOD

Fault Tolerant Full adder/ subtractor using Reversible Gates [11]: Reversible logic gates are popular for the up and coming future computing advancements. Reversible logic is rising as a vital research territory having its application in differing fields, for example, low power CMOS plan.

This is the technique for outlining full Adder/Subtractor circuit utilizing fault tolerant reversible logic gates.

The outline can work separately as a reversible Full Adder/Subtractor unit. It is an equality safeguarding reversible adder cell, that is, the equality of the information sources coordinates the equality of the yields. Equality checking is one of the generally utilized mistake recognition components in computerized logic and information correspondence frameworks. This is on account of a large portion of the number juggling functions isn't equality protecting. This equality safeguarding reversible adder can be utilized to integrate any arbitrary Boolean function. It permits any fault that influences close to a solitary flag promptly perceptible at the circuit's essential yields. The fault tolerant Half Adder/Half Subtractor utilizes two Feynman Double Gates and two Fredkin Gates.

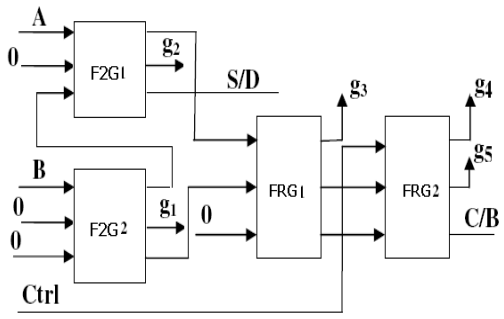

Fig.1: Fault Tolerant Half Adder / Half Subtractor

By associating two Fault Tolerant Half Adder/Half Subtractor we will develop the Fault Tolerant Full Adder/Full Subtractor as appeared in the figure 2.3. Fault Tolerant Half Adder/Half Subtractor contains four steady information sources and five garbage yields.

Garbage yield alludes to the yield that isn't utilized for encourage calculations. Reversible logic execution of adder circuit has been considered by a few creators and has been exhibited that a reversible adder circuit can be acknowledged with no less than two garbage yields and one steady info.

This prerequisite isn't the same for fault tolerant reversible adder circuit. Since in a fault tolerant adder circuit the information equality must matches the equality of the yields.

For configuration full adder/subtractor circuit the regular approach is taken after, that is utilizing two half adder circuits. The two half adder circuits are associated in course frame with a Feynman Double Gate which shapes the Full Adder/Full Subtractor as appeared in the figure underneath.

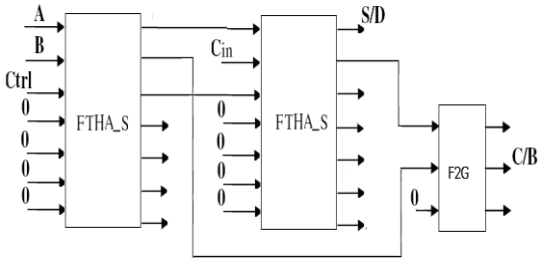

Fig.2:Fault Tolerant Full Adder / Full Subtractor

The full adder/subtractor using proposed FTHA_S circuit is shown in the fig 2.13
The expression for full adder & full subtractor is:
Sum = A ^ B ^ C
Carry ((A ^ B)&C) ^ (A & B)
Borrow = (~A & B) + (B & Bin) + (Bin & (~ A))
From above we can say that the expressions for sum and difference are same. The only difference lies in the carry and borrow expressions.
There are three sources of info A, B, Cin and a control line ctrl which controls its method of activity.

At the point when control flag ctrl is at logic 0, the circuit goes about as full adder and when ctrl goes to logic 1, the circuit performs subtraction. The aggregate and distinction line appeared as S/D and its convey and acquire flag is spoken to by C/B. Whatever remains of nine consistent sources of

info are compelled to logic 0 though there are eleven garbage signals. This fault tolerant full adder/subtractor (FTFA) circuit can perform expansion and subtraction with the utilization of just single ctrl.

It utilizes the Feynman twofold door and Fredkin entryway which isn't just reversible yet additionally has property of equality saving. Reversible circuits are those circuits that don't lose data and reversible calculation in a framework can be performed just when the framework includes reversible gates. Reversible logic door is a n-input n-out logic gadget with balanced mapping.

This decides the yields from the information sources and furthermore the data sources can be remarkably recuperated from the yields. A reversible circuit ought to be composed utilizing least number of reversible logic gates. The reversible logic tasks don't eradicate (lose) data and disperse less warmth.

Disadvantages of the Existing Method

There are many disadvantages in the existing method they are given below,

- More number of gates are required :
  It requires nine reversible logic gates (5 Feynman Double gates & 4 Fredkin gates).
- More number of constant inputs :
  It has total nine constant inputs.
- More numbers of Garbage Outputs :
  It has 11 Garbage outputs (outputs which are required only to satisfy the reversibility principle).
- More power dissipation :
  Power dissipation is also more.

To overcome the drawbacks of this method we have implemented a new design called “Optimal Design of Reversible Parity Preserving New Full Adder/ Full Subtractor”.

It requires less number of gates, less constant inputs and less garbage outputs when compared to the existing methods.

III. PROPOSED WORK

In every digital circuit the basic components are N-Bit Adders and N-Bit Multipliers. In this the basic element is 1-Bit Adder. If we worked to implement 1- Bit Adder efficiently then it indirectly helps for the optimistic design of any Digital circuit. This paper proposes a circuit which works as a Full Adder and full Subtractor. Its symbol is shown Fig. 3. And Truth Table is shown in Table I.

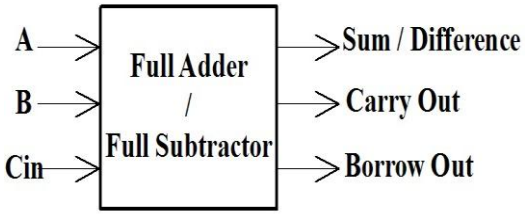

Fig .3: Basic Symbol of Full Adder/Full Subtractor

TABLE I
Truth Table of Full Adder/ Full Subtractor

Inputs			Outputs		
A	B	C_{in}	Sum/ Difference	C_{out}	B_{out}
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	1	1	1

A full adder is a combinational circuit that includes 3 input bits and produces 2 yields. In the 3 input bits 2 bits are information bits and other piece is past stage convey. The 3 input factors are indicated by A, B and Cin. The yields total and convey are meant by 'S' and 'Cout'. The scientific condition speaking to the full adder is A+B+Cin.

A full subtractor is a combinational circuit that subtracts 2 input bits from first information and produces 2 yields. In the 3 input bits 2 bits are information bits and other piece is available stage obtain. The 3 input factors are indicated by A, B and Cin (for accommodation reason display organize get is meant by Cin). The yields Difference and Borrow are meant by 'D' and 'Session'. The numerical condition speaks to full subtractor is A-B-Cin.

Here, in this proposed strategy we are actualizing both full adder and full subtractor in a solitary circuit. At that point, as indicated by this usage the articulation for expansion and subtraction is same.

What's more, for convey yield and get yield there will be two unique articulations.

The Boolean expressions of Full Adder / Full Subtractor are

Sum / Difference = A ^ B ^ Cin Carry out (Cout) = ((A ^ B) & Cin) + (A & B)

Borrow out (Bout) = ((A ~^ B) & Cin) + (A & B)

The carry out and borrow out expressions can be modified and rewritten as

Carry out (Cout) = ((A ^ B) & Cin) ^ (A & B)

Borrow out (Bout) = ((A ~^ B) & Cin) ^ (A & B)

Reversible logic adder circuits which are implemented earlier by several authors are not fault tolerant (Peres gate) i.e., the parity of input and parity of output is not same. This paper describes the fault tolerant Full adder/ Full subtractor with minimal garbage outputs and constants inputs. We have many reversible gates, some of them are given below.

A.Feynman Double Gate

Feynman Double gate[6] is also one of the basic reversible logic gate with 3 inputs and 3 outputs also represented as 3*3 gate. It is depicted in Fig4 along with truth table in Table II. The inputs are denoted by I (A, B, C) and outputs are denoted by O (P, Q, R).

The relation between inputs and outputs are given by

$$P = A$$
$$Q = A \wedge B$$
$$R = A \wedge C$$

Quantum cost of a Feynman double gate is 2.

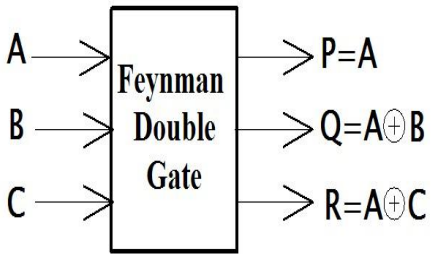

Fig .4: Feynman Double Gate

The truth table of Feynman Double Gate which contains three inputs and three outputs is as shown below.

TABLE II

Truth Table of Feynman Double Gate

Inputs			Outputs		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

B.Fredkin Gate

Fredkin gate[5][7] is also one of the basic gate of reversible logic gate with 3 inputs and 3 outputs and denoted by 3*3 gate. It is depicted in Fig.5 along with truth table in Table III. The inputs are denoted by I (A, B, C) and outputs are denoted by O (P, Q, and R)

The relationship between inputs and outputs is given by

$$P = A$$
$$Q = (\sim A \& B) \wedge (A \& C)$$
$$R = (\sim A \& C) \wedge (A \& B)$$

For Fredkin gate the quantum cost is 5.

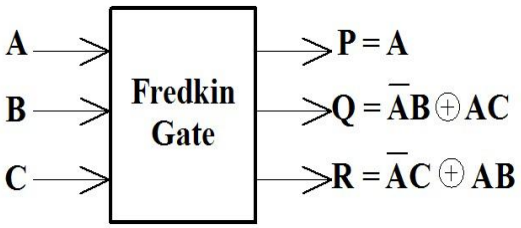

Fig .5:Fredkin Gate

The truth table of Fredkin Gate is as shown in the table below

TABLE III

Truth Table of Fredkin Gate

Inputs			Outputs		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

C.Toffoli Gate

Toffoli gate[5][9] is also one of the basic reversible logic gates with 3 inputs and 3 outputs. It also called as 3*3 gate. It is depicted in Fig 3.4 along with truth table in Table IV For a Toffoli gate, the inputs are denoted by I (A, B, C) and outputs are denoted by O (P, Q, R).

The relationship between inputs and outputs is

P=A

Q=B

R= (A&B) ^ C

The QC of a Toffoli gate is 5

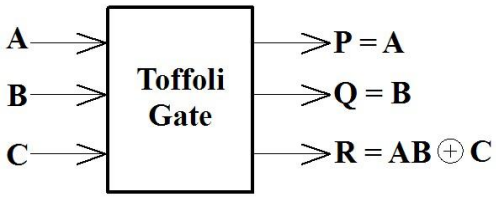

Fig .6: Toffoli Gate

The truth table of the Toffoli Gate is as shown in the figure

TABLE IV
Truth Table of Toffoli GatePeres Gate

Inputs			Outputs		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Peres gate[8] is also one of the basic reversible logic gate with 3 inputs and 3 outputs also denoted as 3*3 gate. It is depicted in Fig 3.5. Along with truth table in Table 3.5. The inputs are denoted by I (A, B,C) and outputs are denoted by O(P, Q, R).

The relationship between inputs and outputs is given by

P = A

Q = A ^ B

R = (A&B) ^ C;

For Peres gate the QC is 4

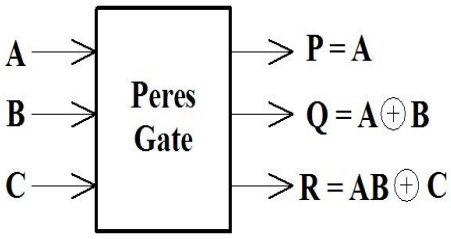

Fig .7: Peres Gate

The truth table of the Peres Gate is as shown in the table below

TABLE V
Truth Table of Peres Gate

Inputs			Outputs		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Among the above reversible logic gates we are using Feynman Double gate and Fredkin gate for efficient design. To implement the full adder/subtractor we are using 3 Feynman double gates and one Fredkin gate. The circuit diagram for the design of Reversible Parity Preserving New Full Adder/ Full Subtractor is as shown in the figure below.

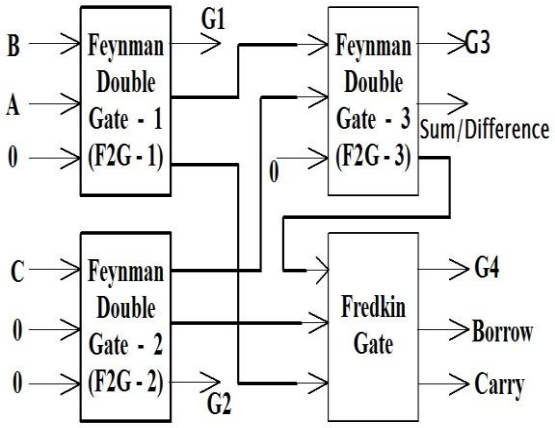

Fig .8:Full adder/ subtractor using Parity conserving reversible gates

For the main Feynman twofold entryway (F2G-1) the data sources are B and An and one consistent info '0'. By utilizing this first Feynman twofold entryway we are copying the B' info and A^B is produced. One 'B' yield act like garbage yield (G1). Presently, the yields for the primary Feynman Double Gate are G1, B^A, B^0.

For second Feynman twofold door (F2G-2) the sources of info are 'C' and 2 steady information sources '0'. The second Feynman twofold entryway (F2G-2) is utilized to triplicate the Cin. For this reason Cin,'0','0' are connected as contributions to second Feynman twofold entryway (F2G-2) and it delivers all yields as Cin. Among three yields one of the Cin demonstrations like garbage yield (G2). Presently the yields of the Feynman Double Gate 2 are C, C^0, C^0.

For third Feynman twofold entryway (F2G-3), the data sources are B^A i.e., yield of first Feynman twofold door (F2G-1), C i.e., yield of second Feynman twofold door (F2G-2) and one steady information '0' at that point the yields are B^A (garbage yield G3), A^B^C i.e., SUM/DIFFERENCE and A^B.

The A^B (yield of third Feynman twofold door (F2G-3)), C^0 (yield of second Feynman twofold entryway (F2G-2)), B^0 (yield of first Feynman twofold entryway (F2G-1)) are connected as contributions to the Fredkin door. The yields are A^B (garbage yield G4), BORROW out and CARRY out.

D.Block Diagram showing Reversibility:

Reversible logic is also a core part of the quantum circuit model. The parity preserving (Conserving) reversible logic gates are one class of reversible logic gates that have unique property of fault tolerance derived from parity conservation techniques. Thus they can be efficiently made use to design fault tolerant arithmetic circuits.Reversible computation in a system can be performed only when the system comprises of reversible gates.

Here in this proposed design we used two reversible gates. The symbol of Optimized Parity Preserving Full Adder / Full Subtractor is shown in Fig 3.7

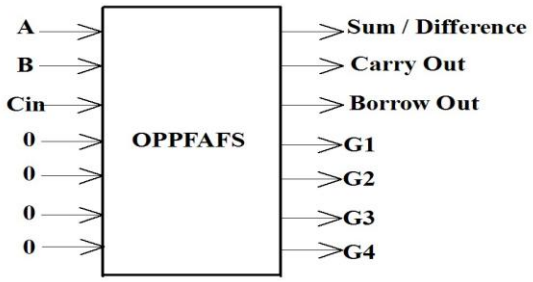

Fig .9: Symbol of Full Adder / Full Subtractor using Reversible Parity Conserving gate

Inputs and outputs of the proposed design are shown in the figure above. It contains A, B, Cin as inputs and Sum/Diff Carry Out and Borrow Out as outputs along with the four constant inputs and four garbage outputs. The outputs which are used only to maintain the reversible property are called garbage outputs. These garbage outputs are unwanted outputs or not useful outputs. Garbage outputs are maintained at a rate of heavy price.

Secondly, the input output patterns have one to one correspondence. Lastly, the circuit must be acyclic. In addition to these a circuit is called reversible if the outputs are applied at the output then inputs are reproduced at the input i.e., we are reproducing the inputs from outputs. The fault tolerant reversible gates are special gates in reversible gates. The fault tolerant gates satisfies the property of parity preserving i.e., the parity of input and output is same.

A logic block is called parity preserving if every gate in that is parity preserving [4]. If a logic block is implemented with fault tolerant gates then those gates will not require extra circuitry to check errors which occur in computation or communication.

An N*N reversible gate can be represented as

Iv = (I1,I2,I3,I4,……IN)

Ov = (O1,O2,O3,……ON).

Where Iv and Ov represent the input and output vectors respectively.

The following circuit also satisfies the reversibility principle i.e., explained in Fig 3.8. In the diagram two OPPFAFS (Optimal design Parity Preserving reversing Full Adder/ Full Subtractor) are considered. They are OPPFAFS-1 and OPPFAFS-2. The inputs are applied to the OPPFAFS-1. The outputs of OPPFAFS-1 are

connected to OPPFAFS-2 across its output. Thus OPPFAFS-2 is going to reproduce the inputs. Hence it satisfies reversibility principle.

The block diagram showing reversibility (for the proposed design) is shown in the figure below.

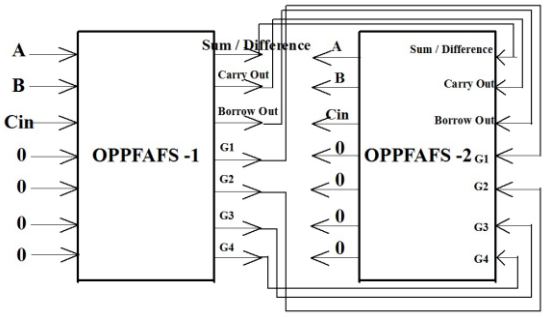

Fig.10: Block diagram showing reversibility

A logic block is called parity preserving if every gate in that is parity preserving [4]. If a logic block is implemented with fault tolerant gates then those gates will not require extra circuitry to check errors which occur in computation or communication.

Advantages of Proposed method

- Less number of gates are required
  It has total 4 reversible gates (3 Feynman Double gates and 1 Fredkin gate).
- Less number of constant inputs.
  It has 4 constant inputs i.e., decreased almost half when compared to existing method.
- Less numbers of Garbage Outputs.
  It has 4 garbage outputs in total i.e., decreased almost half when compared to existing method.
- Less complex.
  As the number of gates, constant inputs decreases complexity of the design also decreases.
- Power dissipation is very low compared to existing method.
- Less delay when compared to existing method.
- Quantum cost is low compared to existing method.

Applications

- Used in quantum computing.
- Used in low power VLSI circuits.
- Used in optical computing.
- Used to synthesize any arbitrary Boolean functions.
- Used to detect errors and It allows any fault that affects no more than a single signal readily detectable at the circuit's primary outputs.
- Used in Nanotechnology for shrinking the size of the transistor.

IV.RESULTS

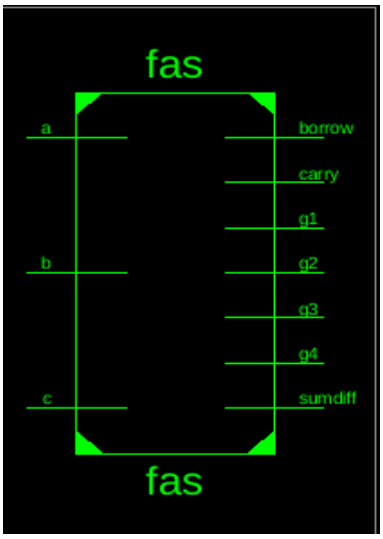

Fig.11:Block Diagram

This is the RTL schematic diagram for Optimal Design of Reversible Parity Preserving New Full Adder / Full Subtractor. Here a, b, c are the 3 inputs and sumdiff, carry, borrow, are the outputs and the remaining are the garbage outputs i.e., g1, g2, g3, g4.

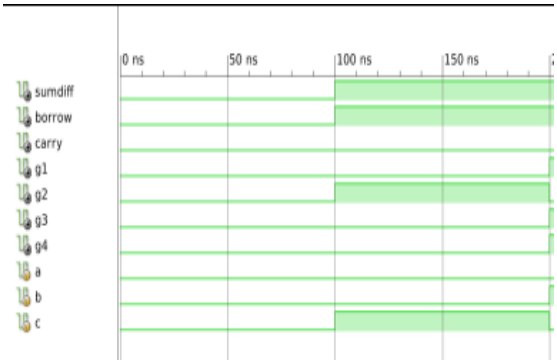

Fig.12: Output Waveform

The proposed display is simulated utilizing Xilinx ISE 14.7 utilizing Verilog code. The execution parameters like power, entryway check, garbage yields, steady data sources and quantum cost for proposed demonstrate are demonstrated as follows. In, fault tolerant Full adder/Full Subtractor is proposed and there is a change of half power, half door tally, 63% garbage yields, 55% consistent sources of info and 56% quantum cost than the proposed display. In, just fault tolerant Full adder is proposed and there is a change of 20% power, 33%

door tally, 33% garbage yields, 20% steady data sources and 40% quantum cost than the proposed display. Thus, the proposed model of full adder/full subtractor is giving preferred execution over said existing models. The comparision of the proposed technique with the current strategy is appeared in the accompanying table.

TABLE VI

Power Analysis of proposed Design:

Static power (mw)	Dynamic Power (mw)	Total power (mw)
13.66	0	13.66

Delay for the proposed design:

The delay time for the proposed design is 6.702 ns

TABLE VII

Comparision of Proposed and Existing Methods

FULL ADDER/ FULL SUBTRACTOR	Gate Count	Constant Inputs	Garbage Outputs	Quantum Cost
[10] Existing method	09	09	11	25
Proposed method	04	04	04	11

V. CONCLUSION

This task center basically around usage of a model which can be worked as full adder and additionally full subtractor with better execution. Here a structure is proposed with equality monitoring gates which diminishes testing equipment. The reversible logic idea work proficiently if number of garbage yields, steady sources of info and quantum cost is low. The power scattering is significantly lessened if the reversible logic circuits are executed with quantum gates. On the off chance that we do that then we can spare power, cash and additionally nature.

Power consumption is one of the significant restricting component in VLSI plan. The broadly utilizing CMOS innovation actualizing with irreversible logic will hit a scaling limit past 2020 and the real constraining variable is expanded power scattering. The irreversible logic is supplanted by reversible logic to diminish the power dissemination. The gadgets actualized with reversible logic gates will have interest for the up and coming future computing advancements as they devours less power.

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