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Carry Select Adder design using Brent Kung Adder

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ABSTRACT
Adders are the basic building blocks in digital integrated circuit based designs. Ripple Carry Adder (RCA) gives the most compact design but takes longer computation time. The time critical applications use Carry Look-ahead scheme (CLA) to derive fast results but they lead to increase in area. Carry Select Adder is a compromise between RCA and CLA in term of area and delay. Delay of RCA is large therefore it is replaced with parallel prefix adder which gives fast results. Carry Select Adder (CSA) architectures are proposed using parallel prefix adders. Instead of using dual Ripple Carry Adders (RCA), parallel prefix adder i.e., Brent Kung (BK) adder is used to design Regular Linear CSA. Parallel prefix adders are used to speed up the binary additions as they are very flexible. The structure of Carry Look Ahead Adder (CLA) is used to obtain parallel prefix adders. Tree structures are used to increase the speed of arithmetic operation. Parallel prefix adders are used for high performance arithmetic circuits in industries as they increase the speed of operation.
Keywords :— CSLA, Brent kung adder, Parallel prefix Adder, Delay, Power, Area.

I. INTRODUCTION

The layout of ripple carry adder is simple, which allows for fast design time; however, the ripple carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. The gate delay can easily be calculated by inspection of the full adder circuit.

The block diagram of 4-bit Ripple Carry Adder is shown here below :

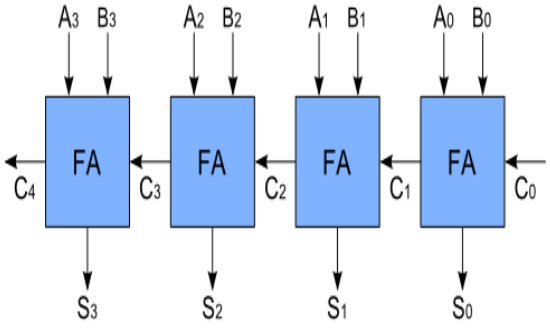


Fig.1 Ripple Carry Adder.

II. CARRY LOOK AHEAD ADDER

To reduce the computation time, there are faster ways to add two binary numbers by using carry lookahead adders. They work by creating two signals P and G known to be Carry Propagator and

Carry Generator. The carry propagator is propagated to the next level whereas the carry generator is used to generate the output carry, regardless of input carry. The block diagram of a 4-bit Carry Look ahead Adder is shown here below :

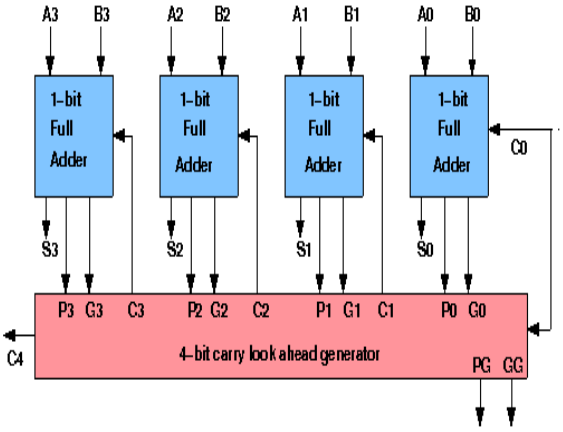


Fig.2 4-Bit Carry Look Ahead Adder

The number of gate levels for the carry propagation can be found from the circuit of full adder. The signal from input carry C_{in} to output carry C_{out} requires an AND gate and an OR gate, which constitutes two gate levels. So if there are four full adders in the parallel adder, the output carry C_5 would have 2 X 4 = 8 gate levels from C_1 to C_5. For an n-bit parallel adder, there are 2n gate levels to propagate through.

III. CARRY SELECT ADDER

In electronics, a carry-select adder is a particular way to implement an adder which is a logic element that computes the (n+1)-bit sum of two n-bit numbers.

The carry-select adder is simple but rather fast, having a gate level depth of O (sqrt n).

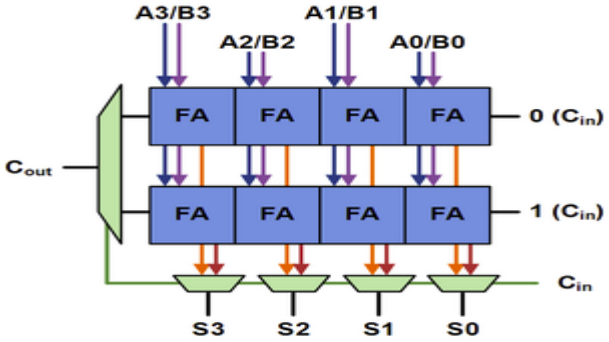


Fig.3 Two 4-Bit Carry Select Adder

Above is the basic building block of a carry-select adder, where the block size is 4. Two 4-bit ripple carry adders are multiplexed together, where the resulting carry and sum bits are selected by the carry-in. Since one ripple carry adder assumes a carry-in of 0, and the other assumes a carry-in of 1, selecting which adder had the correct assumption via the actual carry-in yields the desired result.

IV. BASIC STRUCTURE OF REGULAR SQRT CSLA

The basic square root Carry select adder has a dual ripple carry adder with 2: 1 multiplexer the main disadvantage of regular CSLA is the large area due to the multiple pairs of ripple carry adder. The regular 16-bit Carry select adder is shown in Fig. It is divided into five groups with different bit size RCA. From the structure of Regular CSLA, there is scope for reducing area and power consumption. The carry out calculated from the last stage i.e. least significant bit stage is used to select the actual calculated values of the output carry and sum.

V. MODIFIED SQRT CSLA USING BEC

The modified Carry select adder has a single ripple carry adder with Binary to Excess-I converter, which replace the ripple carry adder with Cin=l, in order to reduce the area and power consumption of the regular CSLA. To replace the n-bit RCA, an n+ I -bit BEC is required .

The Boolean expressions of the 4-bit BEC is listed as (note the functional symbols NOT, & AND, I\XOR).

VI. BINARY TO EXCESS 1 CONVERTER

As stated above the main work is to use BEC instead of the RCA with Cin=1 in order to reduce the area and power consumption of the regular CSLA. To replace the *n*-bit RCA, an *n+1*bit BEC is required. A structure and the function table of a 4-b BEC are shown in Figure and Table

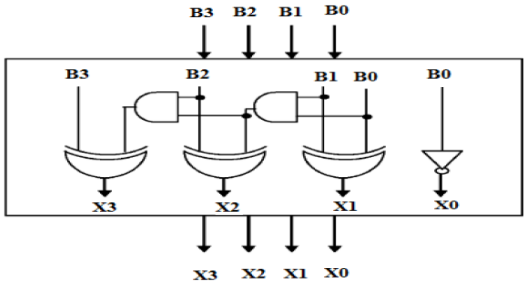


Fig.4 4-Bit BEC

Table 1 Functional Table of 4 Bit BEC

B[3:0]	X[3:0]
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

VII. PARALLEL PREFIX ADDER

Parallel-Prefix Structures

In this paper the ripple carry adder has been replaced by using the parallel prefix adders i.e. Brent Kung adder due to its high speed of operation when cin='0' and when cin='1' ripple carry adder is used.

To resolve the delay of carry-look ahead adders, the scheme of multilevel-look ahead adders or parallel-prefix adders can be employed. The idea is to compute small group of intermediate prefixes and then find large group prefixes, until all the carry bits are computed. These adders have tree structures within a carry-computing stage similar to the carry propagate adder.

VIII. BRENT-KUNG PARALLEL PREFIX NETWORK ADDER

The Brent-Kung adder is a parallel prefix adder. Parallel prefix adders are special class of adders that are based on the use of generate and propagate signals. Simpler Brent-Kung adders was been proposed to solve the disadvantages of Kogge-Stone adders. The cost and wiring complexity is greatly reduced. But the logic depth of Brent-Kung adders increases to 2log (2n-1), so the speed is lower. In 1982, Brent & Kung described this clever.

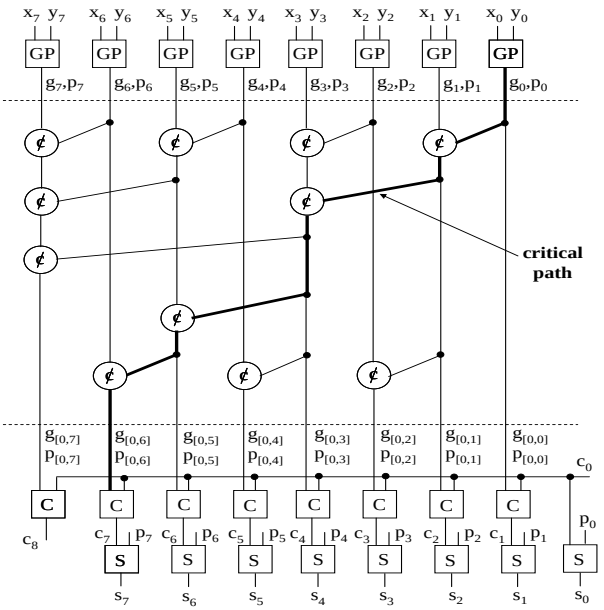


Fig.5 8-Bit Brent-Kung Parallel Prefix Network Adder

Brent-Kung adder is a very well-known logarithmic adder architecture that gives an optimal number of stages from input to all outputs but with asymmetric loading on all intermediate stages. It is one of the parallel prefix adders. Parallel prefix adders are unique class of adders that are based on the use of generate and propagate signals. The cost and wiring complexity is less in Brent kung adders. But the gate level depth of Brent-Kung adders is 0 (log2(n)), so the speed is lower. The block diagram of 4-bit Brent-Kung adder is shown in Fig.

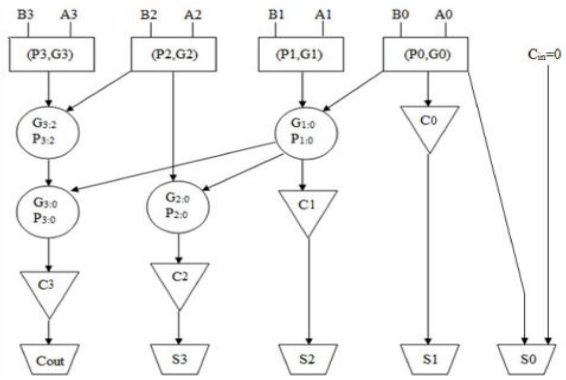


Fig.6 Brent Kung Adder 4bit

IX. IMPLEMENTATION

Conventional Carry Select Adder consists of dual Ripple Carry Adders and a multiplexer. Brent Kung Adder has reduced delay as compared to Ripple Carry Adder. So, Regular Linear BK CSA is designed using Brent Kung Adder. Regular Linear KS CSA consists of a single Brent Kung adder for Cin=O and a Ripple Carry Adder for Cin=1. It has four groups of same size. Each group consists of single Brent Kung adder, single RCA and multiplexer. We use tree structure form in Brent Kung.

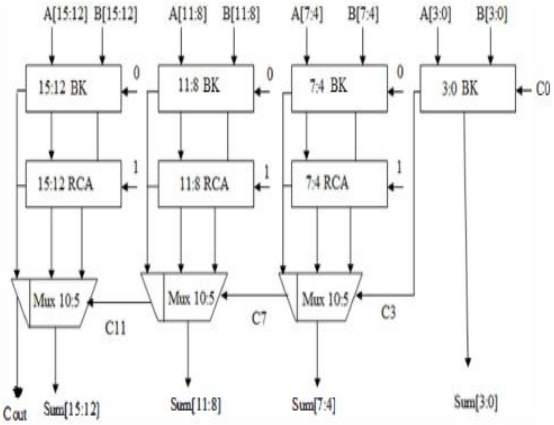
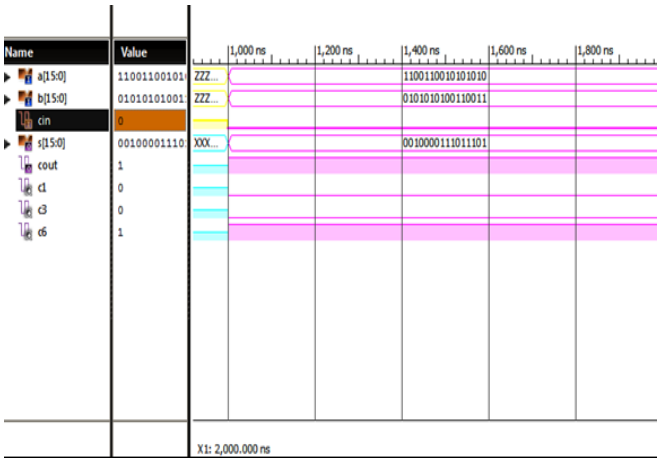


Fig.7 Block Diagram of CSLA Using Brent Kung Adder

In group 2 of Regular Linear CSA, there are single BK for Cin=O and single RCA for Cin=1. Now, the C3 tells whether the input carry is 0 or 1 and depending on its value the output of particular block is selected. If C3=0 then the output of BK with Cin=O is selected using 10:5 multiplexer and if C3=1 then output of RCA with Cin=l is selected using the MUX. A 4-bit Sum [7:4] and an output carry, C7 is obtained at the output of group 2.

X. RESULTS

Simulation:



The inputs of 16 bits a,b are 1100110011001100 and 0101010100110011. Carry is 0.The output of sum is 0010000111011101 and carry out is 1.The ripple carries of C1,C3,C6 are 0,0,1.

Comparison of Delay, Power and Area for Adders:

Table 2 Comparison of Delay, Power and Area for Adders

Adder Name	LUT's	Delay(ns)
Modified SQRT CSLA	127	22
CSLA using BEC	59	13.737
Regular SQRT CSLA using BK	40	2.88

XI. CONCLUSIONS

In this paper carry select adder using Brent Kung has been designed and implemented successfully using Xilinx ISE software. As, parallel prefix adders derive fast results therefore Brent Kung adder is used. Carry select adder with dual ripple carry adders has been replaced with Brent Kung adder when cin='0' for high speed of operation and less delay.

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