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Design of Low Power, High-Performance 2-4, and 4-16 Mixed-Logic Line Decoders

A. Pradeep Kumar, K. Mounika
Assistant Professor, PG student, Department of Electronics and Communication Engineering,
JNTU University
Malla Reddy Engineering College, Maisammaguda, Dulapally road, Hyderabad
Telangana - India

ABSTRACT

This paper introduces a mixed-logic design method for line decoders, combining transmission gate logic, pass transistor dual-value logic and static CMOS. Two novel topologies are presented for the 2-4 decoder: a 14-transistor topology aiming at minimizing transistor count and power dissipation and a 15-transistor topology aiming at high power- delay performance. Both a normal and an inverting decoder are implemented in each case, yielding a total of four new designs. Furthermore, four new 4-16 decoders are designed, by using mixed-logic 2-4 pre-decoders combined with standard CMOS post-decoder. All proposed decoders have the full swinging capability and reduced transistor count compared to their conventional CMOS counterparts. Finally, a variety of comparative spice simulations at the 32 nm shows that the proposed circuits present a significant improvement in power and delay, outperforming CMOS in almost all cases.

Keywords :— Line Decoder, Mixed-Logic, Power-Delay Optimization.

I. INTRODUCTION

Static CMOS circuits are utilized for by far most of rationale entryways in coordinated circuits [1]. They comprise of the corresponding nMOS pulldown and pMOS pullup systems and present great execution and in addition protection from commotion and gadget variety. In this manner, CMOS rationale is portrayed by heartiness against voltage scaling and transistor estimating and in this way solid operation at low voltages and little transistor sizes [2]. Information signals are associated with transistor doors just, offering diminished plan many-sided quality and help of cell-based rationale amalgamation and outline.

The pass-transistor justification was for the most part created in the 1990s, when different plan styles were presented [3-6], planning to give a suitable contrasting option to CMOS rationale and enhance speed, power and range. Its principle plan distinction is that data sources are connected to both the doors and the source/deplete dispersion terminals of transistors. Pass transistor circuits are executed with either individual nMOS/pMOS pass transistors or parallel sets of nMOS and pMOS called transmission gates.

This work builds up a blended motive plan system for line decoders, consolidating doors of various hypothesis to a similar circuit, with an end goal to get enhanced execution contrasted with the single-style outline. Line decoders are central circuits, generally utilized as a part of the fringe hardware of memory exhibits (e.g., SRAM), multiplexing structures, execution of Boolean principle capacities and different applications. Notwithstanding their significance, a generally little measure of writing is committed to their streamlining, with some current work including [7-9].

This paper is composed of: Section II gives a short diagram of the analyzed decoder circuits, including rationale portrayal and execution with traditional CMOS hardware. Section III presents and portrays the newly blended rationale plans. Section IV leads a relative report among the proposed and regular decoders through legitimate reproduction, with a nitty gritty exchange on the inferred comes about. Section V gives the rundown and last finishes of the work introduced.

II. OVERVIEW OF LINE DECODERCIRCUITS

In computerized frameworks, discrete amounts of data are spoken to by parallel codes. An n-bit double code can tell up to 2n particular components of coded information. A decoder is a combinational circuit that proselytes double data from n input lines to a most extreme of 2n extraordinary yield lines or less, if the n-bit coded data has unused mixes. The circuits inspected in this work are called n-to-m line decoders, and their motivation is to create the m=2n minterms of n input factors.

A.2-4 Line Decoder

A 2-4 line decoder creates the 4 minterms D0-3 of 2 input factors A and B. Its rationale operation is condensed in a table. Contingent upon the information mix, one of the four yields is chosen and set to 1 while the others are set to 0. A modifying 2-4 decoder produces the integral minterms

I0-3, accordingly the chose yield is set to 0, and the rest are set to 1, as appeared in Table II.

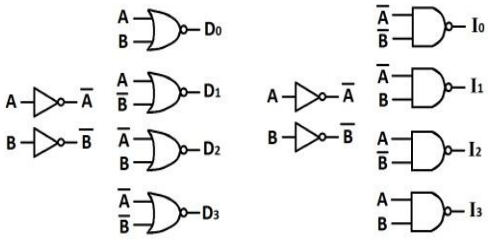
TABLEI:TRUTH TABLE OF 2-4 DECODER

A	B	D 0	D 1	D 2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

TABLEII: TRUTH TABLE OF INV 2-4 DECODER

A	B	I 0	I 1	I 2	I3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

In traditional CMOS plan, NAND and NOR entryways are wanted to and additionally, since they can be executed with four transistors, instead of six, subsequently actualizing rationale capacities with higher effectiveness. A 2-4 decoder can be executed with 20 transistors utilizing two inverters and four NOR entryways, as appeared in Fig.1(a).The comparing modifying actualized with 2-4 decoders and 16 2-input NAND doors (Fig. 2(b)). In CMOS rationale, these outlines require 8 inverters and 24 4-input entryways, yielding a sum of 104 transistors each.



(a) (b)

Fig. 1. 20-transistor 2-4 line decoders actualized with CMOS rationale: (a) Non-transforming NOR-based decoder, (b) Inverting NAND-based decoder. The decoder can likewise be actualized with 20 transistors utilizing two inverters and four NAND entryways, as appeared in Fig. 1(b).4-16

B. Line Decoder with 2-4Pre-decoders

A 4-16 line decoder produces the 16 minterms D0-15 of four input factors A, B, C and D, and a rearranging 4-16 line decoder creates the integral minterms I0-15. A clear use of these circuits would require 16 4-input NOR and NAND entryways. In any case, a more productive outline can be acquired utilizing a pre-decoding strategy, as per which pieces of n address bits can be pre-decoded into 1-of-2n pre-decoded lines that fill in as contributions to the last stage decoder [1]. With this method, a 4-16 decoder can be executed with 2-4 upsetting decoders and 16 2-input NOR can doors (Fig. 2(a)) and an altering one be Fig. 2. 104-transistor 4-16 line decoders executed with CMOS rationale and predecoding:(a)Non-rearranging decoder actualized with two 2-4 altering pre-decoders and a NOR-based post-decoder, (b) Inverting decoder actualized with two 2-4 non-reversing pre-decoders and a NAND-based post-decoder**.**

III. NEWMIXED-LOGICDESIGNS

In combinational rationale, transmission entryways have for the most part been utilized as a part of XOR-based circuits, for example, full adders and as the essential switch component in multiplexers. Be that as it may, we consider their utilization in the execution of AND/OR rationale, as exhibited in [5], which can be proficiently connected in line decoders. The 2-input TGL AND/OR doors gates appear in Fig. 3(a) and 3(b), separately. They are full-swinging, however not reestablishing for all information mixes. Concerning transistor rationale, there are two principle circuit styles: those that utilization nMOS just pass-transistor circuits, as CPL [3] and those that utilization both nMOS and pMOS pass-transistors, as DPL [4] and DVL [6]. The style we consider in this work is DVL, which offers a change on DPL, saving its full swing operation with lessened transistor tally [10].The2-input DVL AND/OR entryways are appeared in Fig. 3(c) and 3(d), individually. Like the TGL doors, they are full-swinging yet non-reestablishing. Accepting that correlative information sources are accessible, the TGL/DVL entryways require just 3 transistors, instead of the 4 required in CMOS NAND/NOR doors. Decoders are high fan out circuits, where a couple of inverters can be utilized by

various entryways, along these lines utilizing the TGL/DVL doors can result to lessened transistor check.

IV. The 14-transistor 2-4 Low-Power Topology

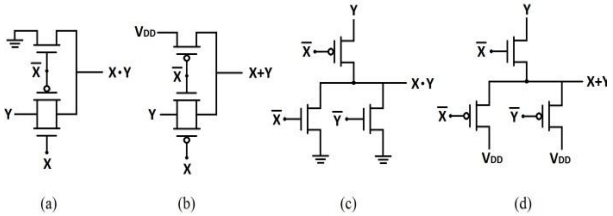


Fig. 3. The 3-transistor AND/OR gates considered in this work (a) TGL AND gate, (b) TGL OR gate, (c) DVL AND gate, (d) DVL OR gate.

A vital regular normal for these entryways is their lopsided nature, i.e. the way that they don't have adjusted info loads. As appeared in Fig. 3, we named the 2 entryway inputs X and Y. In TGL entryways, input X controls the door terminals of all three transistors, while input Y spreads to the yield hub through the transmission entryway. In DVL doors, input X controls two transistor entryway terminals, while input Y controls 1 entryway terminal and spreads through a pass transistor to the yield. We will allude to X and Y contributions as the control flag and the spread flag of the door, separately.

This topsy-turvy highlight gives a fashioner the adaptability to perform flag game plan, i.e. picking which input is utilized as control and which as spread flag in each door. Having an integral contribution as engender flag is not a decent practice, since the inverter added to the proliferation way expands delay fundamentally. Thusly, while executing the hindrance (A'B) or suggestion (A'+B) work, it is more effective to pick the upset variable as control flag. While actualizing the AND (AB) OR (A+B) work, either decision is similarly effective. At long last, while actualizing the NAND (A'+B') or NOR (A'B') work, either decision results to an integral engender flag, perforce.

A. The 14-transistor 2-4 Low-Power Topology

Planning a 2-4 line decoder with either TGL or DVL doors would require an aggregate of 16 transistors (12 for AND/OR entryways and four for inverters). In any case, by blending both AND entryway sorts into a similar topology and utilizing legitimate flag game plan, it is conceivable to dispense with one of the two inverters, in this manner lessening the aggregate transistor check to 14.Let us expect that, out of the two information sources, to be specific An and B, we mean to dispose of the B inverter from the circuit. The Do minterm (A'B') is executed with a DVL entryway, where An is utilized as engender flag. The D1 minterm (AB') is actualized with a TGL door, where B is utilized as spread flag. The D2 minterm (A'B) is executed with a DVL entryway, where A is utilized as propagating signal. At long last, The D3 minterm (AB) is actualized with a TGL entryway, where B is utilized as proliferate flag. These specific decisions totally turn away the utilization of the correlative B flag, hence the B inverter can be dispensed with from the circuit bringing about a 14-transistor topology (9 nMOS, 5 pMOS).

Following a practically identical strategy with OR entryways, a 2-4 annoying line decoder can be realized with 14 transistors (5 nMOS, 9 pMOS), additionally: I0, I2 are executed with TGL (using B as multiply banner) and I1, I3 are executed with DVL (using A as spread banner). The B inverter can before long be precluded. The inverter transfer diminishes transistor count, reliable effort and general trading activity of the circuits, along these lines restricting power dispersing. To the degree the makers are concerned, 14 is the base number of transistors required to comprehend a full-swinging 2-4 line decoder with static (non-coordinated) method of reasoning. The two new topologies are named '2-4LP' and '2-4LPI', where 'LP' stays for 'low power' and 'I' for 'disquieting'. Their schematics are showed up in Fig. 4(a) and Fig. 4(b), independently.

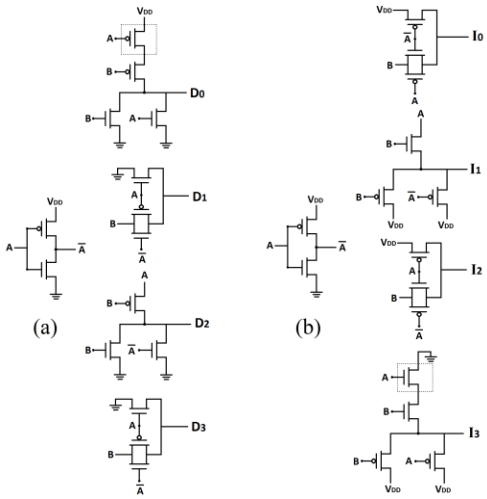


Fig. 4. New 14-transistor 2-4 line decoders: (a) 2-4LP (b) 2-4LPI.

B. The 15-transistor 2-4 High-Performance Topology

The low-control topologies displayed above have a downside in regards to most pessimistic scenario in the delay, which originates from the utilization of correlative An as the proliferate motion on account of D0 and I3. Be that as it may, acknowledging D0 and I3 can be actualized all the more proficiently by utilizing standard CMOS entryways, since there is no requirement for correlative signs. In particular, D0 can be executed with a CMOS NOR entryway and I3 with a CMOS NAND door, adding one transistor to every topology. The new outlines coming about because of this adjustment blend 3 unique sorts of rationale into a similar circuit and present a noteworthy change in delay while just somewhat expanding power dissemination. They are named '2-4HP' (9 nMOS, 6 pMOS) and '2-4HPI' (6 nMOS, 9 pMOS), where 'HP' remains for 'superior' and 'I' for 'transforming'. The thinking behind the 'HP' assignment is that these decoders exhibit both low power and low defer qualities, in this manner accomplishing a general decent execution. The 2-4HP and 2-4HPI schematics are appeared in Fig. 5(a) and Fig. 5(b), individually, where the extra transistors are featured for less demanding refinement.

C. Integration in 4-16 Line Decoders

At a little scale, circuits in light of pass transistor rationale can understand rationale capacities with less transistors and enhanced execution contrasted with static CMOS. Be that as it may, falling a few non-reestablishing circuits causes a quick corruption in execution. A blended topology approach, i.e. substituting reestablishing and non-reestablishing levels of rationale, can conceivably convey ideal outcomes, consolidating the positive describes of both.

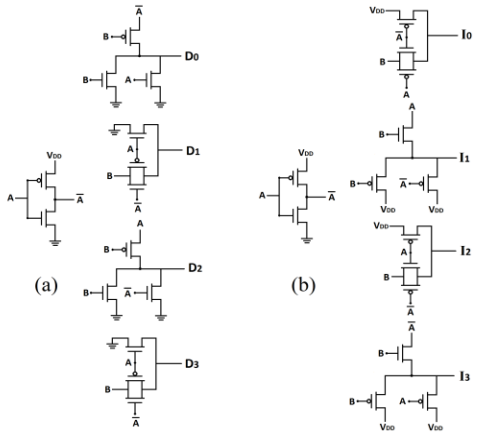


Fig. 5. New 15-transistor 2-4 line decoders: (a) 2-4HP (b) 2-4HPI.

Receiving this plan procedure, and as for the hypothesis exhibited on segment II, we actualized four 4-16 decoders by utilizing the four new 2-4 as predecoders in conjunction with CMOS NOR/NAND entryways to create the decoded yields. The new topologies got from this blend are: 4-16LP (Fig. 6(a)), which joins two 2-4LPI predecoders with a NOR-based post-decoder, 4-16HP (Fig. 6(b)), which consolidates two 2-4HPI predecoders with a NOR-based post-decoder, 4-16LPI (Fig. 6(c)), which consolidates two 2-4LP predecoders with a NAND-based post-decoder and, at long last, 4-16HPI (Fig. 6(d)), which consolidates two 2-4HP pre-decoders with a NAND-based post-decoder.

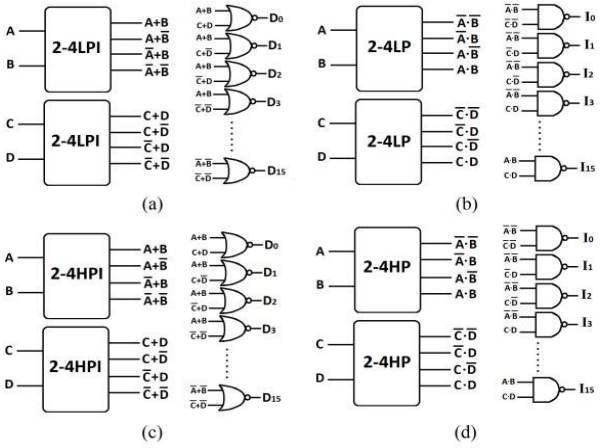


Fig. 6. New 4-16 line decoders: (a) 4-16LP, (b) 4-16LPI, (c) 4-16HP, (d) 4- 16HPI.

The 'LP' topologies have a sum of 92 transistors, while the 'HP' ones have 94, instead of the 104 transistors required by the unadulterated CMOS execution.

IV. SIMULATION RESULTS

Every one of the reproductions are performed on Microwind and DSCH. The fundamental concentration of this work is to address all difficulties faces in outlining of Decoder circuit utilizing blended rationale. This work builds up a blended motivational outline procedure for line decoders, consolidating doors of various rationale to a similar circuit, with an end goal to get enhanced execution contrasted with the single-style plan. The reproduction comes about are appeared beneath figures.

Table: 1 Comparisons results of mixed-logic line decoders

DESIGN	PARAMETERS	
	NO.OF TRANSISTORS	POWER
2to4 Decoder CMOS	6T	7.315uw
2to4 Decoder Mixed Logic	8T	6.647uw
4to16 Decoder CMOS	6T	7.315uw
4to16Decoder Mixed Logic	8T	6.647uw

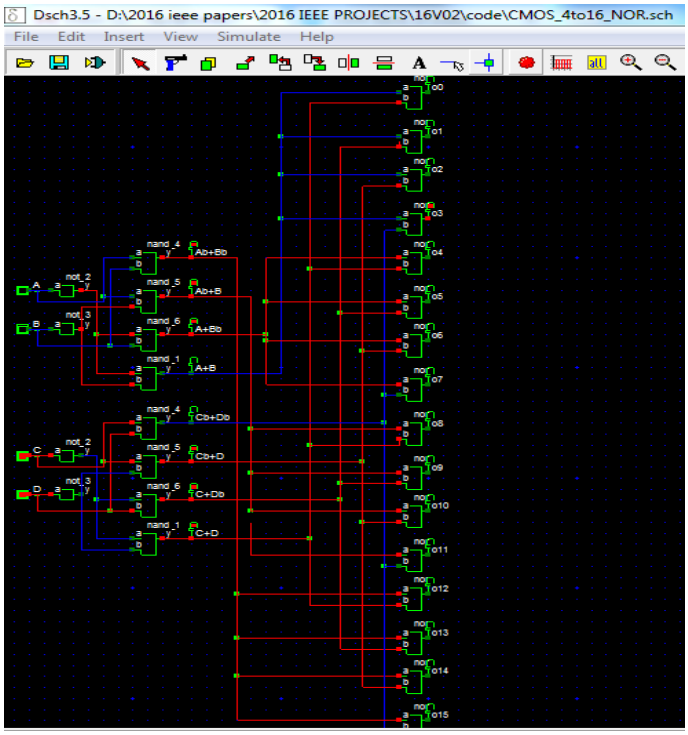


Fig 7: Schematic of 4to16 Decoder Using CMOS

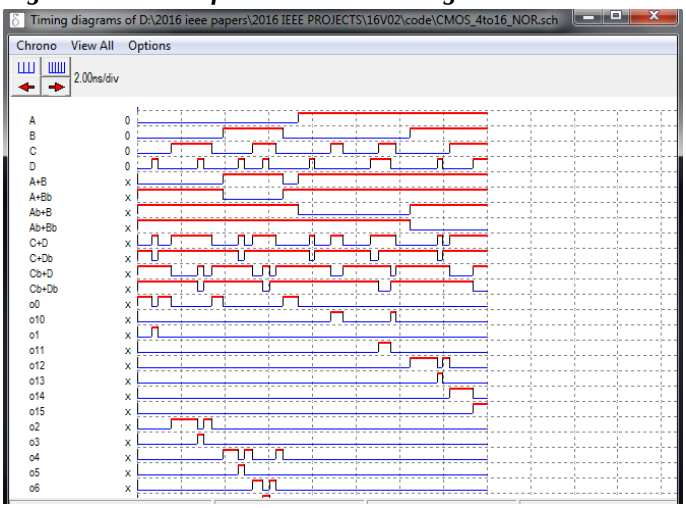


Fig 8: Timing Diagram of 4to16 Decoder Using CMOS

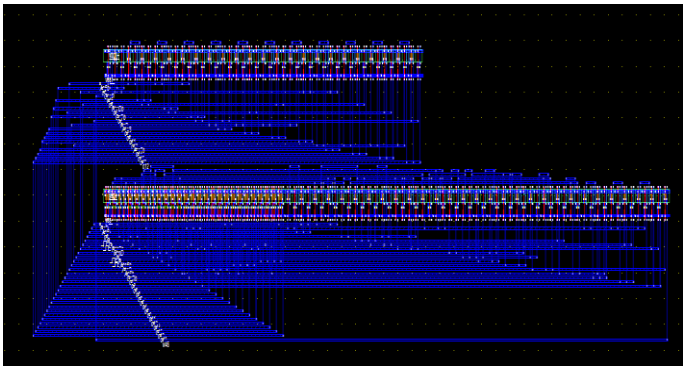


Fig 9: Layout of 4 to 16 Decoder Using CMOS

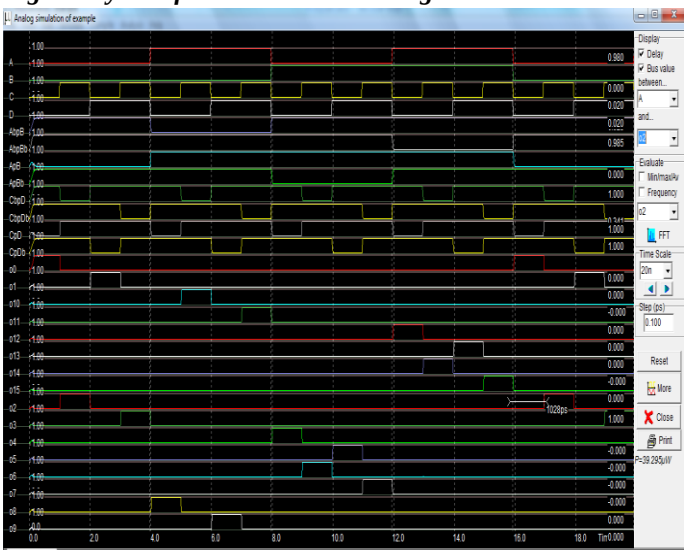


Fig 10: Simulation of Layout of 4 to 16 Decoder Using

CMOS

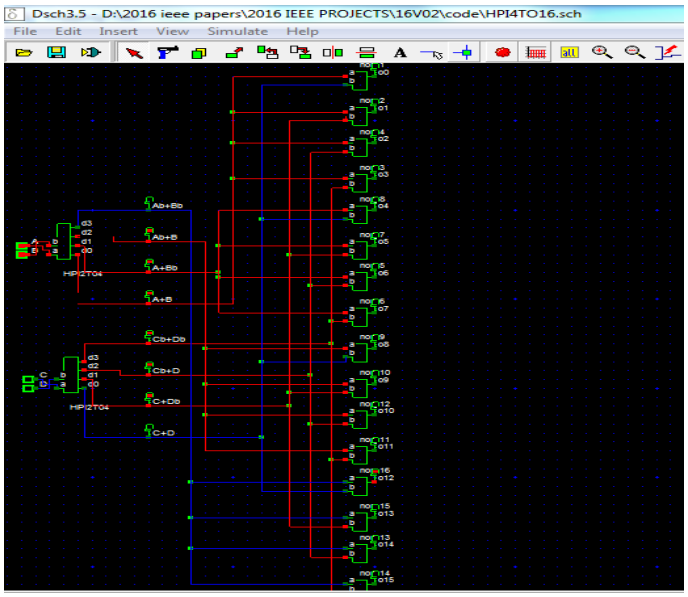


Fig 11: Schematic of 4to16 Decoder Using HPI

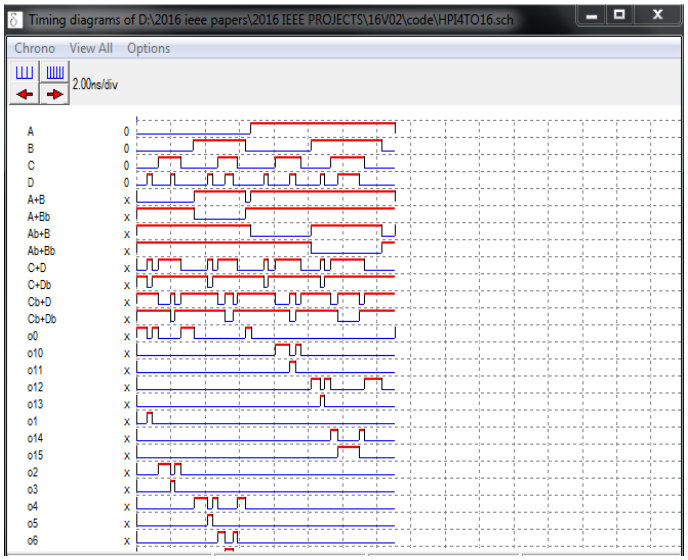


Fig 12: Timing Diagram of 4to16 Decoder Using HPI

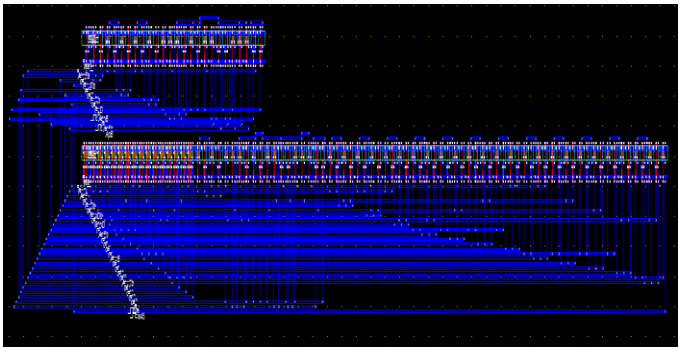


Fig 13: Layout of 4 to 16 Decoder Using HPI

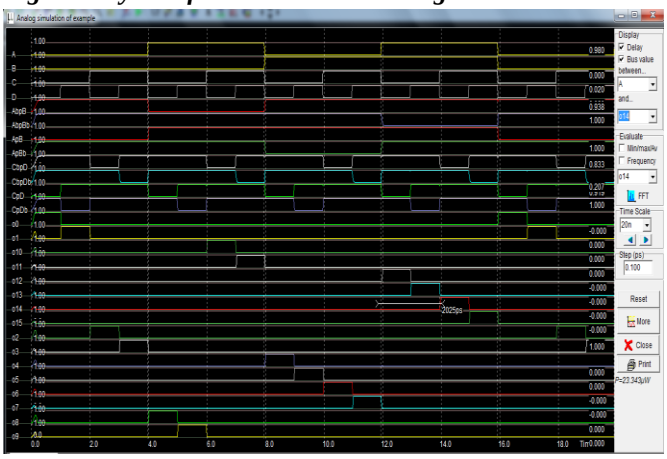


Fig 14: Simulation of Layout of 4 to 16 Decoder Using HPI

V.CONCLUSION

This paper presented a productive blended rationale plan for decoder circuits, joining TGL, DVL and static CMOS. By utilizing this procedure, we created four new 2-4 line decoder topologies, to be specific 2-4LP, 2-4LPI, 2-4HP and 2-4HPI, which offer decreased transistor check (along these lines possibly littler format territory) and enhanced power-postpone execution in connection to regular CMOS decoders.

Moreover, four new 4-16 line decoder topologies were displayed in particular 4-16LP, 4-16LPI, 4-16HP and 4-16HPI, acknowledged by utilizing the blended explanation of 2-4 decoders as pre-decoding circuits and consolidating them with post-decoders executed in static CMOS principle. These outlines consolidate the enhanced execution qualities of pass transistor rationale with the reestablishing ability of static CMOS. An assortment of near zest reproductions was performed at the 32 nm, confirming, as a rule, a distinct preferred

standpoint for the proposed plans. The 2-4LP and 4-16LPI topologies are generally reasonable for applications where range and power minimization is of essential concern. The 2-4LPI, 2-4HP and 2-4HPI, and in addition the comparing 4-16 topologies (4-16LP, 4-16HPI, 4-16HP) ended up being feasible and all-around proficient outlines, in this manner they can viably be utilized as building obstructs in the plan of bigger decoders, multiplexers and other combinational circuits of shifting execution necessities.

Additionally the introduced diminished transistor check and low power attributes can profit both mass CMOS and SOI configuration also. The acquired circuits are to be executed on format level, making them reasonable for standard cell libraries and RTL outline.

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