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A Comparison of Switches and PWM Techniques in Fifteen Level Multilevel Inverter

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ABSTRACT
Nowadays multilevel inverter (MLI) technologies becomes extremely main choice in the area of high power medium voltage energy control. Although multilevel inverter has a number of advantages it has drawbacks in the layer of higher levels because of using large number of semiconductor switches. This may leads to large size and price of the inverter is very high and also increase in losses. So in order to reduce this difficulties in the new multilevel inverter is proposed to reducing the switches. This paper presents the 15-level cascaded multilevel inverter. The proposed 15-level cascaded multilevel inverter is for reducing the total harmonic distortion which is shown in MATLAB/SIMULINK. The switching pattern of semiconductor switches is used to improve the performance of multilevel inverter .so here MCPWM and SVPWM compared in MATLAB/SIMULINK. This scheme reduces the switching loss and also increase the efficiency. To authorize the developed technique simulations are carried out through MATLAB/SIMULINK.

Keywords:- Cascaded Multilevel Inverter, Harmonic Distortion, MATLAB, semiconductor switches, THD, MCPWM, SVPWM

I. INTRODUCTION

Multilevel inverters are becoming recent trends, because of its modularity and simplicity of control to generate particular number of levels. Multilevel inverters have a number of applications such as ups, in power grid, as solar inverter, induction heating and number of other applications. By increasing the number of dc voltage sources, a sinusoidal like waveform can be generated. Thus the total harmonic distortions decreases which has a great significance in power grid applications. A sine wave output is desirable because many electrical products are engineered to work best with a sine wave ac power source. The standard electric utility power attempts to provide a power source that is a good approximation of a sine wave.. Switch mode power supply (SMPS) devices, such as personal computers function on quality of sine wave power. Ac motors directly operated on non-sinusoidal power may produce extra heat, may have different speed-torque characteristics, or may produce more audible noise than when running on sinusoidal power thus the multilevel inverters with reduced number of switches becomes more significant. The multilevel inverters is classified as, neutral point clamped inverters, flying capacitor multilevel inverters and cascade multilevel inverters. Of this three category cascaded multilevel inverter is recent trend because of its reliability. Table1 shows the comparison of conventional multilevel inverters switching components.

Cascaded multi level inverter uses reduced number of power switches and it produces a sinusoidal like waveform. Cascaded multilevel inverter is series connection of power switches and dc voltage sources. Cascaded multilevel inverters have several advantages when compared to other topologies. The main advantages of using the cascaded multilevel inverters are the high power quality waveforms due to the reduction in the total harmonic distortion and also the reduction of dv/dt stresses on the load, cascaded multilevel inverters can be classified as symmetric and asymmetric multilevel inverters. The main difference between symmetric and asymmetric configuration is the magnitude of dc sources. In symmetric configuration magnitudes of dc sources are same, whereas in the asymmetric configuration magnitudes of the dc sources are different. By using the cascaded multilevel inverters desired number of output voltage levels can be obtained by series connection of a number of dc voltage sources. A number of different topologies have been presented in the literature. Numerous basic units are also presented in the literature. The disadvantage of the symmetric configuration is that it requires more number of power switches when compared to the asymmetric configurations. But the dc voltage magnitude is very high in these papers. Single phase and three phase multilevel inverters can be produced by the series connection of a large number of the basic units.

II. CONVENTIONAL SYSTEMS

The cascaded multilevel inverter to generate output of 5 levels using 8 switches, 7

Levels with 12 switches, 9 levels with 16 switches, and so on. Using 4 switch and one dc source for each h-bridge and produces the one level of voltage output which is shown in figure1. Common expression for output voltage Levels, $m = (n + 2)/2$ where n is the number of switches in the inverter. Each Bridge is outputting 3 Levels, $+V$dc, 0, $-V$dc.

The number of levels in the three phase circuit means the output phase voltage and line voltage are 2s+1 and 4s+1 respectively, where s is the number of H-bridges used per phase. For example, Three H- Bridges, Five H-bridges and Seven H-bridges per phase that is 12 switches ,20 switches, and 28 switches per phase are required for 7-level, 11-level and 15-level multilevel inverter respectively. The value of the ac output phase voltage is the sum of the Voltages produced by each H-bridges.

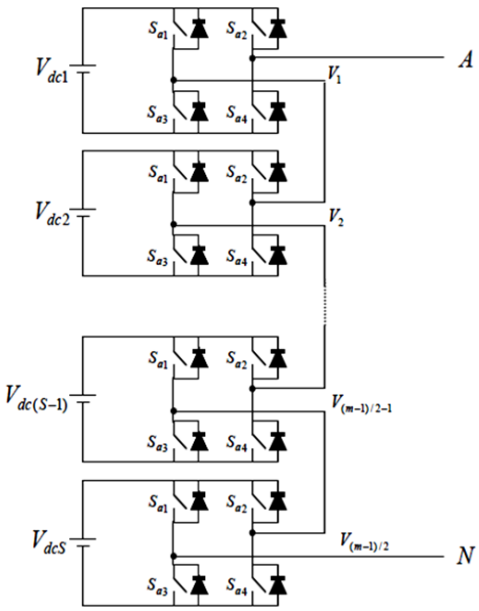


Fig1: conventional cascaded n level multilevel inverter

III. COMPARISON OF SWITCHES

3.1 15 Level MLI With 12 Switches:

This asymmetric 15 level multi level inverter topology is made of 12 switches and 3 dc sources and is shown in Figure 2. One H bridge present in the topology is mainly for voltage level change. The switching scheme is given in Table 1

3.2 15 Level MLI With 10 Switches:

This asymmetric 15 level multi level inverter topology is made of 10 switches and 3 dc sources and is shown in Figure 3. One H bridge present in the topology is mainly for voltage level change. First 6 switches used for level module and H bridge used for voltage shift.

3.3 15 Level MLI With 7 Switches:

multilevel inverter has a common structure of the hybrid multilevel inverter is shown in figure4. Every separate voltage source (1vs, 2vs, 4vs) is associated in series by other sources through a unique circuit connected with it. Every step of the circuit consists of only one active switching element and one bypass diode that make the output voltage as positive one with a number of levels. The basic operation of modified hybrid multilevel inverter for getting the output voltage as +1vdc is to turn on the switch s1 (s2 and s3 turn off) and turning on s2 (s1 and s3 turn off) for getting output voltage as +2vdc. Like wise other levels can be accomplished by turning on the appropriate switches at exacting intervals; table7 shows the basic operation of projected hybrid multilevel inverter.

From The Table It Can Be inferred That Only One H-Bridge Is Connected To Get Both Positive And Negative Polarity. Figure4 And Table 3 Shows The Proposed 15 Level Multilevel Inverter Schematic Diagram And Switching Performance.

- The s number of dc sources and the related number output level can be calculated by using the equation n level =2s+1-1
- Voltage on each step can be calculated by using the equation v=2s-1.vdc
- The number of switches used in this topology is given by the equation n switch=s +4

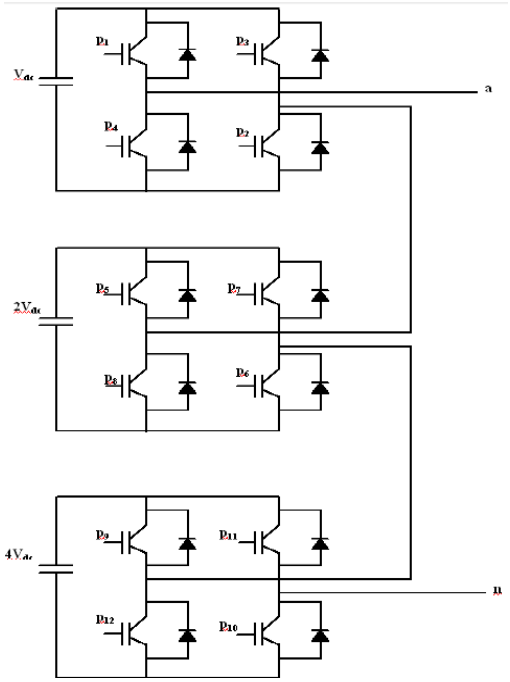


Fig 2. 15 level MLI with 12 switches

. Fig3: 15 level MLI with 10 switches

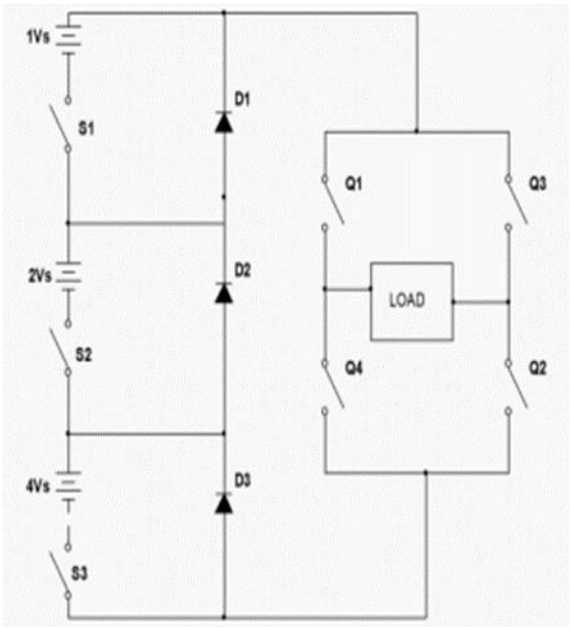
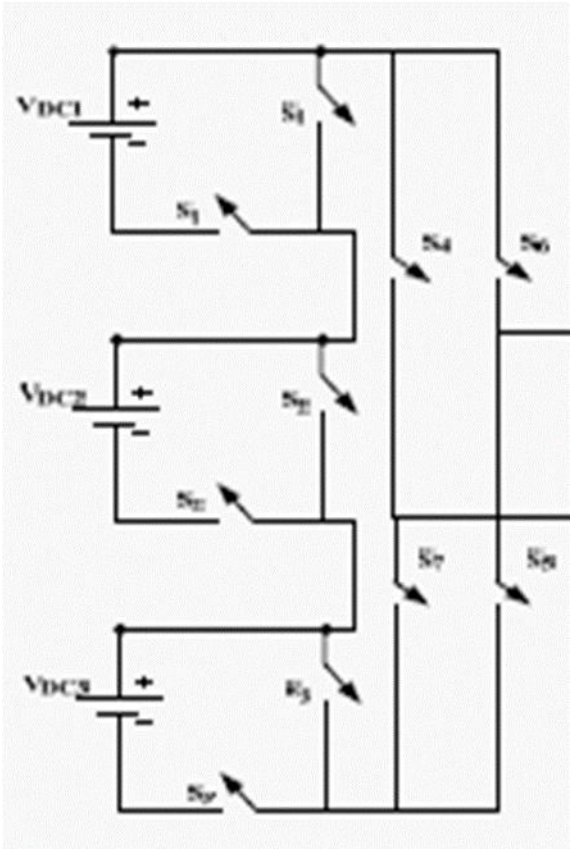


Fig4:15 level MLI with 7 switches



IV. COMPARISON OF MCPWM AND SVPWM

4.1. 15 level MLI with MCPWM technique:

The harmonic content can be reduced by using several pulses in each half cycle of output voltage. The gating signals for turning ON and OFF transistors are generated by comparing a reference signal with a triangular carrier wave. The frequency F_c, determines the number of pulses per half cycle. The modulation index controls the output voltage. This type of modulation is also known as uniform pulse width modulation (UPWM).

Here basic 15 level multi level inverter with 7 switch is using MCPWM technique which was shown in figure4 and waveform of MCPWM shown in figure 4.

4.2.5 level MLI with SVPWM technique:

In steady state, the output of SVPWM is similar to carrier based PWM with a common mode signal added to all three modulation signals of a three-phase PWM inverter. The common mode signal is made up of third harmonics of the supply

frequency (called "triplets"). The output voltage separation is given in figure5. Since the same common mode signal is added to all three phases, the line-line output will not contain the common mode signal. The common mode signal is given by Vcm = max (VA, VB, VC) + min (VA, VB, VC)/2

Switching states												Output voltage
P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	
1	1	0	0	1	1	0	0	1	1	0	0	7Vdc
0	1	0	1	1	1	0	0	1	1	0	0	6Vdc
1	1	0	0	0	1	0	1	1	1	0	0	5Vdc
0	1	0	1	0	1	0	1	1	1	0	0	4Vdc
1	1	0	0	1	1	0	0	0	1	0	1	3Vdc
0	1	0	1	1	1	0	0	0	1	0	1	2Vdc
0	0	1	1	1	1	0	0	0	1	0	1	Vdc
0	1	0	1	0	1	0	1	0	1	0	1	0Vdc
1	1	0	0	0	0	1	1	0	1	0	1	-Vdc
0	1	0	1	1	1	0	0	0	1	0	1	-2Vdc
0	0	1	1	0	0	1	1	0	1	0	1	-3Vdc
0	1	0	1	0	1	0	1	0	0	1	1	-4Vdc
0	0	1	1	0	1	0	1	0	0	1	1	-5Vdc
0	1	0	1	0	0	1	1	0	0	1	1	-6Vdc
0	0	1	1	0	0	1	1	0	0	1	1	-7Vdc

Table1: 15 level 12 switch MLI

Sub- Multilevel Switches						H-bridge Switches				Levels
S_1	S_1'	S_2	S_2'	S_3	S_3'	S_4	S_5	S_6	S_7	V_O
0	0	0	0	0	0	0	0	0	0	0
0	1	1	0	1	0	1	1	0	0	1
1	0	0	1	1	0	1	1	0	0	2
0	1	0	1	1	0	1	1	0	0	3
1	0	1	0	0	1	1	1	0	0	4
0	1	1	0	0	1	1	1	0	0	5
1	0	0	1	0	1	1	1	0	0	6
0	1	0	1	0	1	1	1	0	0	7
0	1	1	0	1	0	0	0	1	1	8
1	0	0	1	1	0	0	0	1	1	9
0	1	0	1	1	0	0	0	1	1	10
1	0	1	0	0	1	0	0	1	1	11
0	1	1	0	0	1	0	0	1	1	12
1	0	0	1	0	1	0	0	1	1	13
0	1	0	1	0	1	0	0	1	1	14

Table 2: 15 level 10 switch MLI switching pattern

S.NO	Intervals	On switches	Off switches	Voltage levels	Current flow path
1	I	S1	S2,S3	+1Vs	S1,D2,D3
2	II	S2	S1,S3	+2Vs	S2,D1,D3
3	III	S1,S2	S3	+3Vs	S1,S2,D3
4	IV	S3	S1,S2	+4Vs	D1,D2,D3
5	V	S1,S3	S2	+5Vs	S1,D2,D3
6	VI	S2,S3	S1	+6Vs	D1,S2,S3
7	VII	S1,S2,S3	-	+7Vs	S1,S2,S3
8	VIII	-	S1,S2,S3	0	D1,D2,D3

Table3: 15 level 7 switch MLI switching pattern

5. Simulation Circuit:

In The Proposed 15 Level MLI ,The Circuit Is Built Of 7 MOSFET Unidirectional Switches. It Can Also Be Built With 3 Unidirectional 4 Bidirectional Switches. The Load Is Resistive With A Value Of 100 Ohm. Three Asymmetric DC Input Voltages Are Used Having The Values Are 48V, 96V And 192V.Figure8 Shows The Simulation Circuit Of Proposed Topology. Note That In Order To Obtain The Shaped 15-Level Output Without Distortion, MOSFET Block Parameters In MATLAB Should Vary According To The Load. Here For 100 Ohm Resistive Load MOSFET Block Parameters Are Set As Follows:

- FFT Resistance=0.1ohm
- Internal Diode Resistance=0.01ohm

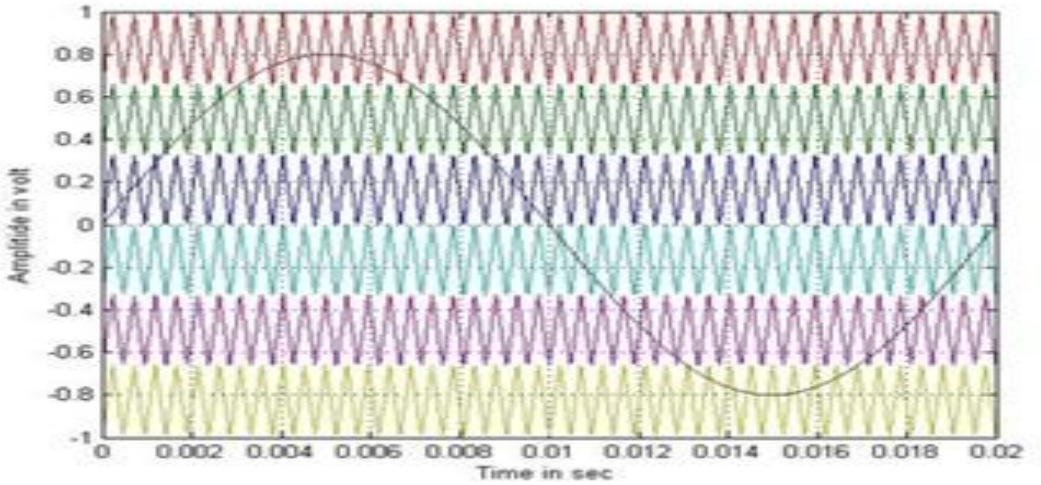


Fig 5: MCPWM waveform

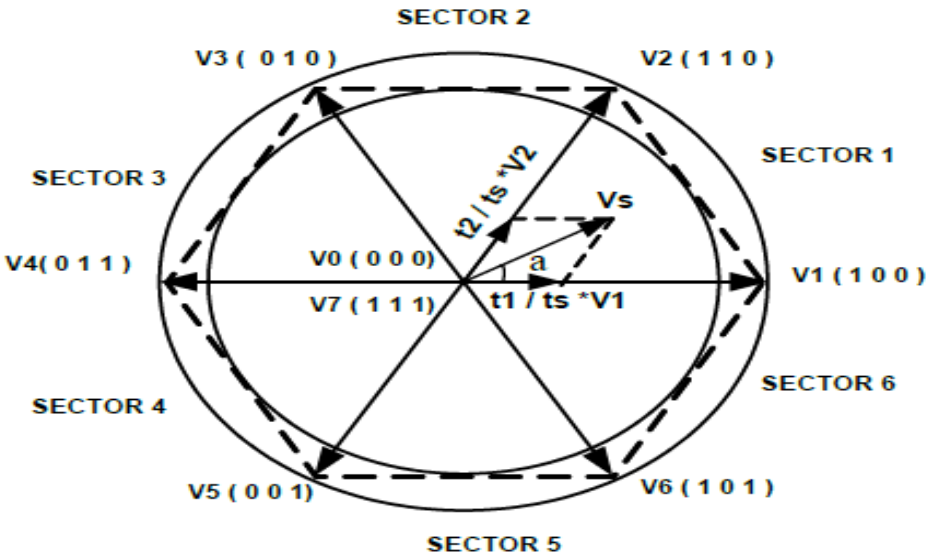


Fig6: SVPWM Vector Estimation

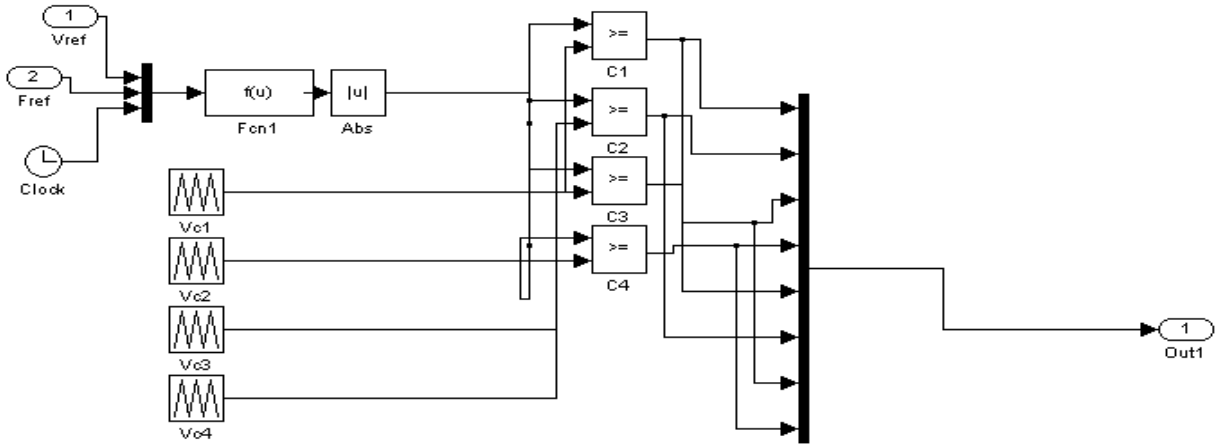


Fig7: Pulse Generation Circuit For MCPWM

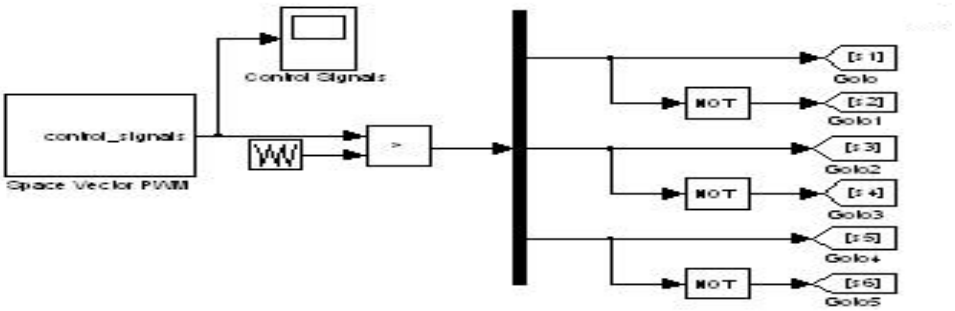


Fig8: Pulse Generation Circuit For SVPWM

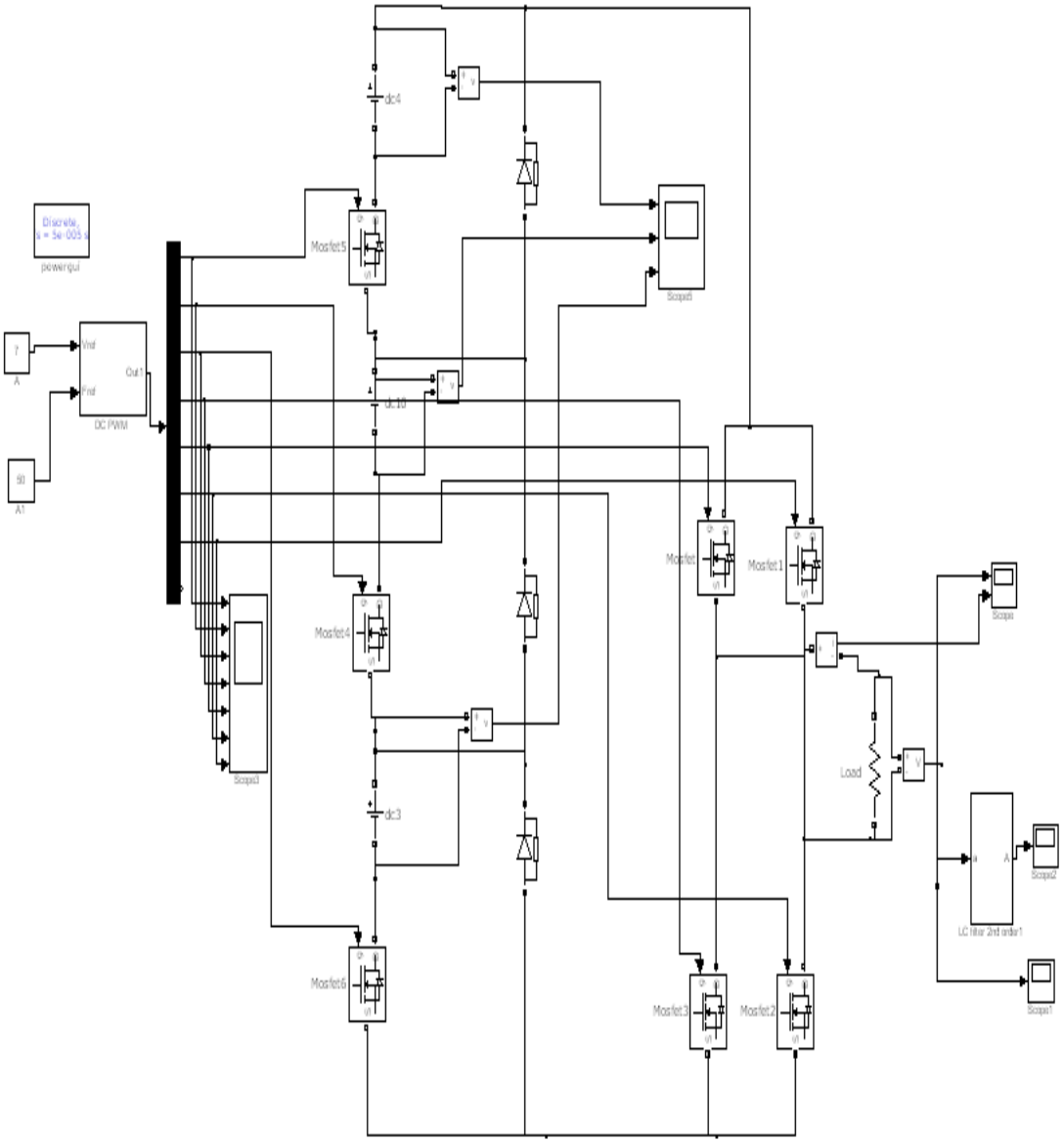


Fig9: 15 Level 7 Switch MLI Simulation Circuit

V. PULSE GENERATION CIRCUIT

Sinewave voltage is compared with different types of triangular waves to obtain the gate pulses. The relational operators are used. The pulse width of the pulses required determines the value of the constants. Pulse width is determined by the on time of each switch and these signals are used for switching the MOSFETS. There are four subsystems in this circuit. The comparator compares the triangular and sinewave which gives the required PWM signals. Pulse generation circuit is shown in figure 7

VI. SPACE VECTOR PULSE GENERATION CIRCUIT

Space vector PWM is an advanced technique used for variable frequency drive

applications. It utilizes dc bus voltage more effectively and generates less THD in the Three Phase Voltage Source Inverter. SVPWM utilize a chaotic changing switching frequency to spread the harmonics continuously to a wide band area so that the peak harmonics can be reduced greatly. Simulation has been carried out by varying the modulation index between 0 and 1. And switching in SVPWM shown in table4 and it is shown in figure8.

Voltage vectors	Switching vectors			Line to neutral voltage			Line to line voltage		
	A	B	C	V_{an}	V_{bn}	V_{cn}	V_{ab}	V_{bc}	V_0
V_0	0	0	0	0	0	0	0	0	0
V_1	1	0	0	2/3	-1/3	-1/3	1	0	-1
V_2	1	1	0	1/3	1/3	-2/3	0	1	-1
V_3	0	1	0	-1/3	2/3	-1/3	-1	1	0
V_4	0	1	1	-2/3	1/3	1/3	-1	0	1
V_5	0	0	1	-1/3	1/3	2/3	0	-1	1
V_6	1	0	1	1/3	-2/3	1/3	1	-1	0
V_7	1	1	1	0	0	0	0	0	0

Table4: switching pattern for SVPWM technique

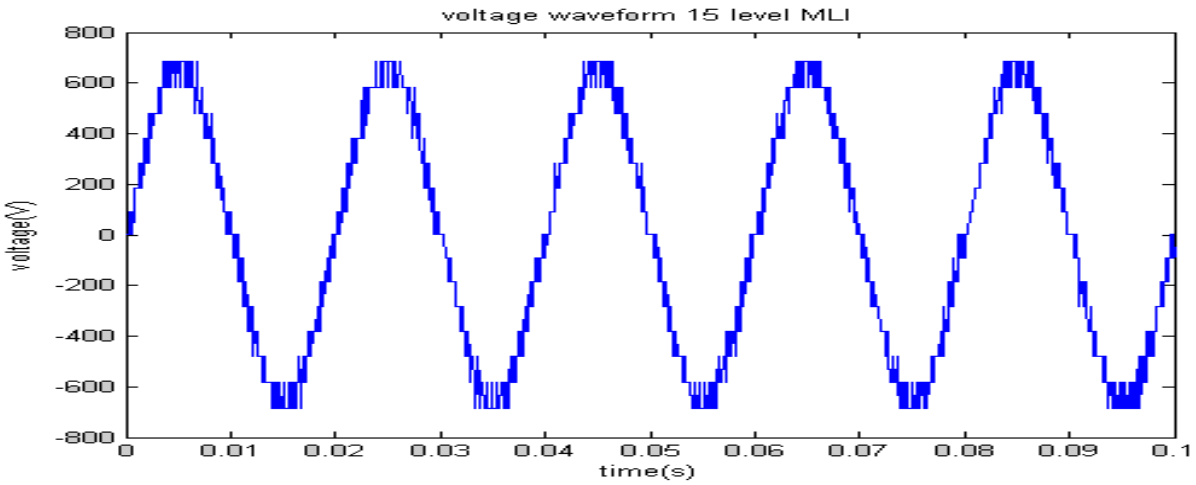


Fig10 : 15 level voltage waveform

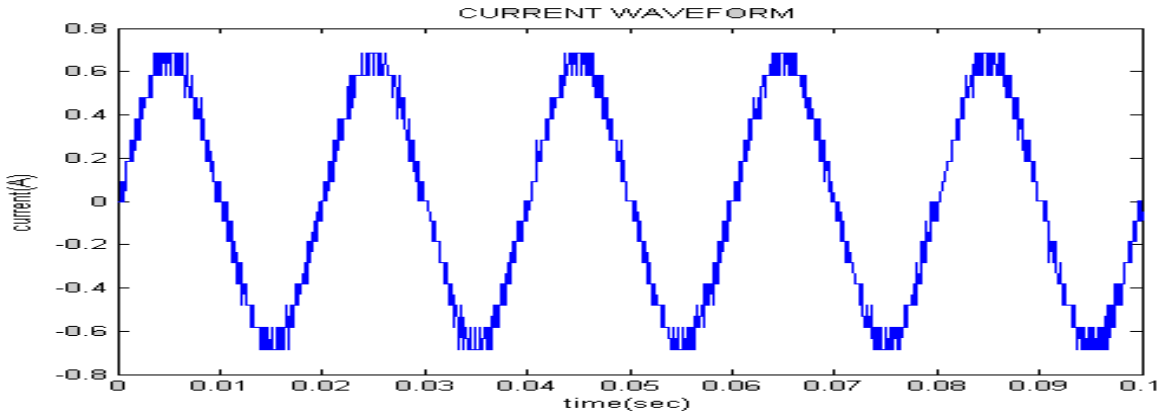


Fig11: 15 level current waveform

6. Simulation Results

The 15 level current and voltage waveform shown in figure 10 and 11. And FFT analysis of 12 switch, 10 switch and 7 switch in MCPWM and SVPWM are shown in figure 12, 13, 14, and 15. And at last table 5 is shown the comparison of THD analysis.

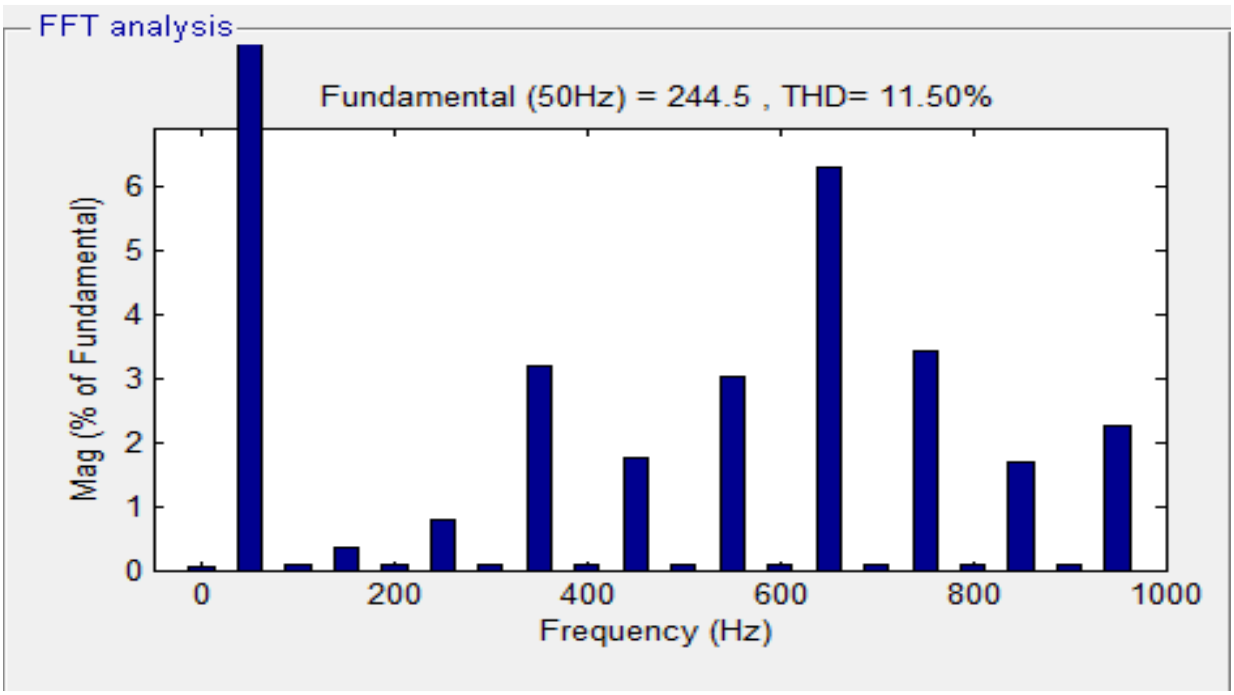


Fig12: FFT analysis of 15 level 12 switch MLI

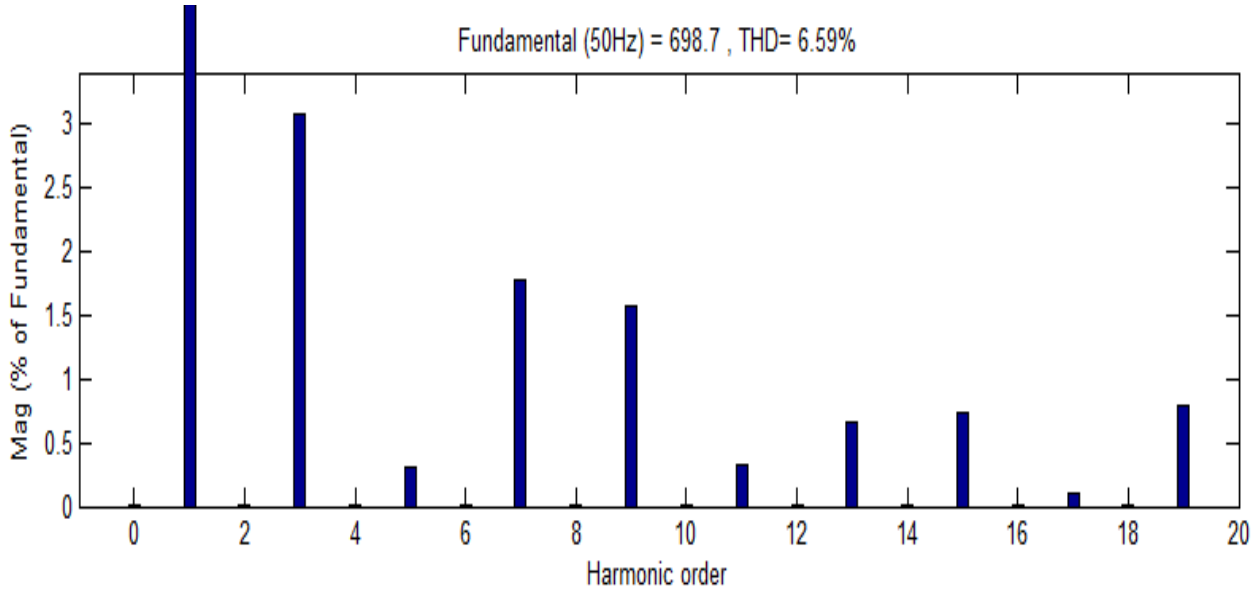


Fig13: FFT analysis of 15 level 10 switch MLI

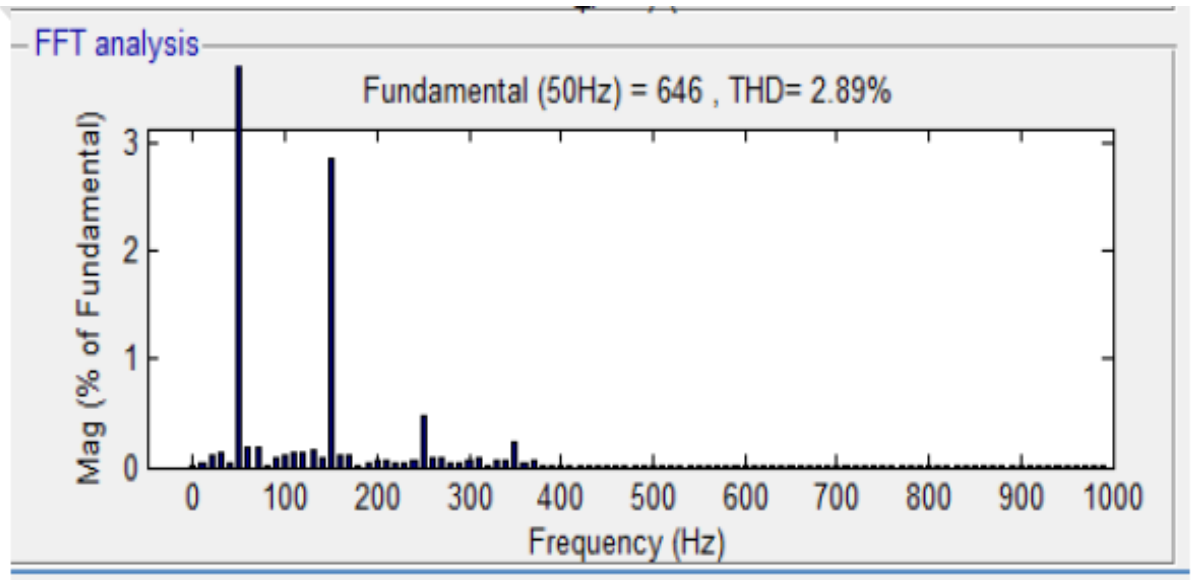


Fig14: FFT analysis of 15 level 7 switch MLI with MCPWM

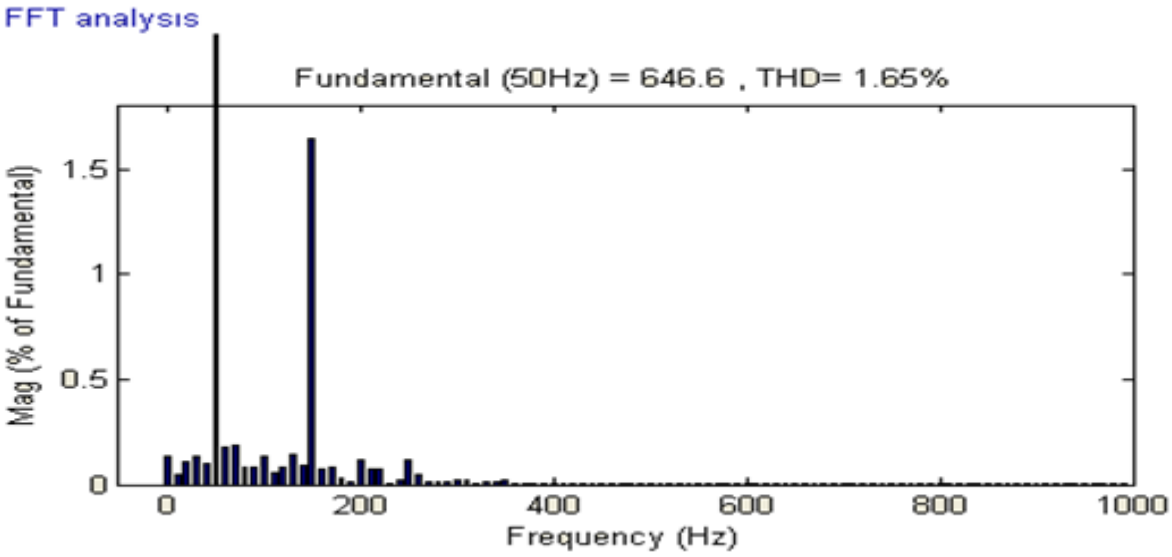


Fig15: FFT analysis of 15 level 7 switch MLI with SVPWM

Configuration	15 level 12 switch	15 level 10 switch	15 level 7 switch	
			MCPWM	SVPWM
THD	11.50	6.59	2.89	1.65

Table 5: comparison of THD

VII. CONCLUSION

In this projected paper, fifteen level asymmetric cascaded multilevel inverter is presented for low harmonics which was produced by SVPWM. The projected inverter can create high quality output voltage close to sinusoidal Waves. It is used to provide improved performance than the conventional cascaded Multilevel inverter. And also this proposed method is used to minimize the switching losses. The total harmonic distortion (THD) can be supplementary reduced.

REFERENCES

[1] K. Gopakumar, Haitham Abu-Rub, P. P. Rajeevan and K.Sivakumar. (2013) "A Nine-Level Inverter Topology for Medium-Voltage Induction Motor Drive With Open-End Stator Winding" IEEE transactions on industrial electronics,vol.60, no.9.

[2] S. Umashankar, T. S. Sreedevi, V. G.Nithya, and D. Vijayakumar (2013) "A New 7-Level Symmetric Multilevel Inverter with Minimum Number of Switches Hindawi Publishing Corporation ISRN Electronics Volume 2013

[3] T. V. V. S. Lakshmi, N. George, S. Umashankar, and D. P.Kothari, "Cascaded seven level inverter with reduced number of switches using level shifting PWM technique," in *International Conference on Power, Energy and Control (ICPEC '13)*, pp. 676–680, February 2013.

[4] J. J. Nedumgatt, D. Vijayakumar, A. Kirubakaran, and S.Umashankar, "A multilevel inverter with reduced number of switches," in *Proceedings of the IEEE Students' Conference on Electrical, Electronics and Computer Science (SCEECS '12)*, pp.1–4, March 2012.

[5] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies,

controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, pp. 724-738, 2002.

[6] N. S. Choi, J. G. Cho, and G. H. Cho, "A general circuit topology of multilevel inverter," in *Proc. IEEE PESC'91*, 1991, pp. 96–103

[7] R Naveen Kumar. Energy Management system for Hybrid RES with Hybrid Cascaded Multilevel inverter. *International Journal of Electrical and ComputerEngineering (IJECE)*. 2014; 4(1): 24~30.

[8] D Mohan, Sreejith B Kurub. *Performance analysis of SPWM control strategies using 13 level cascaded MLI*. IEEE international conference on advances in engineering science &management (ICAESM). 2012.

[9] RH Baker, LH Bannister. Electric Power Converter. *U.S. Patent* 3 867 643. 1975.

[10] FZ Peng. A generalized multilevel inverter topology with self-voltage balancing. *IEEE Trans. Ind. Applicat.*, 2001; 37: 611-618.

[11] J. S. Lai and F. Z. Peng, "Multilevel converters-A new breed of power converters,"*IEEE Trans. Ind. Applicat.*, vol. 32, pp. 509-517, May/June 1996.

[12] kshay K. Rathore, Joachim Holtz, and Till Boller, "Generalized Optimal Pulse Width Modulation of Multilevel Inverters for Low-Switching-Frequency Control of Medium-Voltage High-Power Industrial AC Drives," *IEEE Trans. Ind. Electron.*, vol. 60, Oct. 2013.

[13] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium voltage multilevel converters—State of the art, challenges and requirements in industrial applications," *IEEE Trans. Ind. Electron.*, vol. 57, Aug. 2010.

[14] Muhammad. H. Rashid, Power Electronics Circuits, Devices and Applications, Third Edition, Person Prentice Hall, pp.40-6430, 2004.

[15] Rodriguez J, Lai JS, Peng FZ. Multilevel inverters: survey of topologies, controls, and applications. IEEE Trans Ind Appl 2002;49(4):724–38.

[16] T.F. Wu, H.S. Nien, C.L. Shen, T.M. Chen, "A single-phase inverter system PV power injection and active power filtering with nonlinear inductor consideration," IEEE Transactions on Industry Applications, Vol. 41, No. 4, pp. 1075–1083, Jul./Aug. 2005.

[17] S.J. Park, F.S. Kang, M.H. Lee, C. Kim, "A new single-phase five level PWM inverter employing a deadbeat control scheme," IEEE Transactions on Power Electronics, Vol. 18 No. 3, pp. 831–843, May 2003

[18] S.C¸ amur, B.Arifo˘glu, E.Bes¸er, E.Kandemir Bes¸er, "Harmonic analysis of an improved single phase five level inverter," Wseas Transactions on Power System, Vol. 1, No.2, pp 387-392, Feb. 2006.

[19] K. Sudheer Kumar, E. Mohan, CH. Rajesh Kumar, K. Lakshmi Ganesh, "New Multilevel Inverter Topology with Reduced Switching Devices for Hybrid Electric Vehicles"

[20] Madhav D. Manjrekar, Peter K. Steimer and Thomas A. Lipo, "Hybrid Multilevel Power Conversion System: A Competitive Solution for High-Power Applications".