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Design Of An Efficient Low Power Shift Register Using Double Edge Triggered Flip-Flop

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ABSTRACT
Firstly the shift registers are implemented using single edge triggered flip flop but in the single edge triggered flip flop not efficient. So we go to double edge triggered flip flop and make comparison with single edge and existing double edge triggered flip flops. In the double edge triggered flip flop load does not increase too much .To overcome this problem we go to the clock branch sharing implicit pulse method. This is efficient for the deduction of power consumption and number of transistors.
Keywords: - Flip-Flop, Double edge C2MOS Latch-MUX, Shift Register, CBS_IP.

I. INTRODUCTION

In the digital system and VLSI the clock system is most important. The data transmission in the with respect to the clock system. The clock may be synchronous and asynchronous. The clk system and flip flops are most power consuming elements, that power consumption may be 30-60% by reducing power consumption of on flip flop it will great impact on the total power consumption of the shift register. The power consumption may be occurred with the various sources of power dissipation are switching power (Switching), short circuit power (Pshort-circuit), static power (Pstatic) and leakage power (Pleakage) . The following equation describes the total power consumption (Ptot) related to these four power components

Ptot = Pswitching+Pshortcircuit+Pstatic+Pleakage

The power consumption in the VLSI can be reduced by voltage scaling and double edge triggering flip flop .by using voltage scaling power consumption is reduced whenever the voltage low .if the voltage increases above the threshold value the power consumption in the circuit will be started. So we the technique of double edge triggering. In the single edge triggering data will transmitted only for the positive half cycle. But in the double edge triggering flip flop gives responses for both positive half cycle and negative half cycle. So number of clock transistors and power consumption will be reduced.

II. LATCHES AND FLIP FLOPS

Latches and *flip-flops* are the basic elements for storing information. One latch or flip-flop can store one bit of information. The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately when their inputs change. Flip-flops, on the other hand, have their content change only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. After the rising or falling edge of the clock, the flip-flop content remains constant even if the input changes. There are basically four main types of latches and flip-flops: SR, D, JK, and T. The major differences in these flip-flop types are the number of inputs they have and how they change state. For each type, there are also different variations that enhance their operations.

A. D FLIP FLOP:

A commonly desired function in D flip-flops is the ability to hold the last value stored rather than load in a new value at the clock edge. This is accomplished by adding an enable input called *EN* or *CE* (clock enable) through a multiplexer as shown in Figure 13(a). When *EN* = 1, the primary *D* signal will pass to the *D* input of the flip-flop, thus updating the content of the flip-flop. When *EN* = 0, the bottom AND gate is enabled and so the current content of the flip-flop, *Q*, is passed back to the input, thus, keeping its current value. Notice that changes to the flip-flop value occur only at the

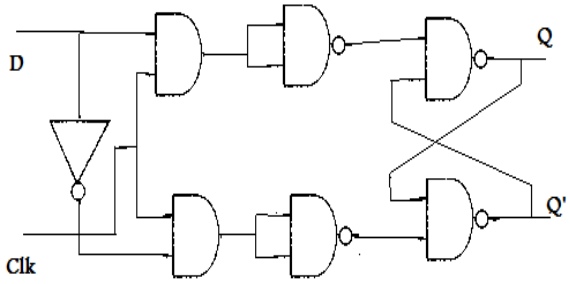

Fig.1: Single Edge Flip-flop

rising edge of the clock. The truth table and the logic symbol for the D flip-flop with CLOCK is shown in respectively

In this above figure represents the single edge triggered flip flop delay will be more and power consumption.

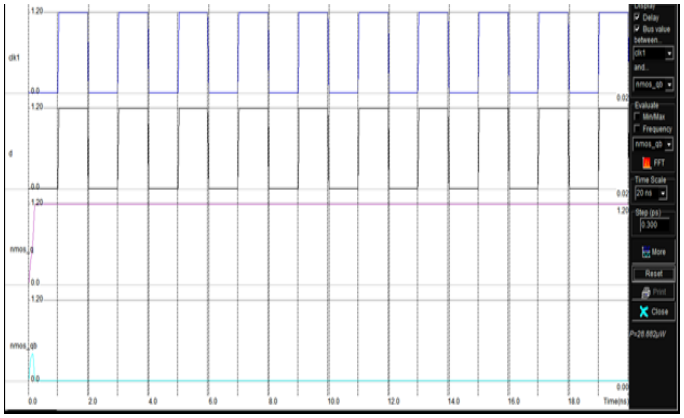

Fig.2: SEFF Simulation Wave form

III. EXISTING DOUBLE EDGE C2MOS LATCH-MUX:

The C2MOS latch-MUX (C2MOSLM) [6], Fig. 2 (a), is dual-edge version of the *C2MOS* master-slave latch . The latch used in the C2MOS LM is the conventional clocked CMOS latch. The multiplexer consists of two clocked CMOS inverters, high-Z-wired at the output, and a buffer inverter. During the time when CLK=0, the forward path of the transparent latch M1-M2, the feedback path of the opaque latch M9-M10 , and the path of the multiplexer M7- M8 are ON. Similarly, during the time when CLK=1 , the forward path of the transparent latch M11-M12 , the feedback path of the opaque latch M3-M4, and the path of the multiplexer – are ON. The C2MOSLM exploits this property of latch-MUX structure to share the clock transistors. In Fig.2(a), only one pair of clocked transistors (M14/M15 or M13/M16) is used for forward path of one latch, feedback path of the other latch, and multiplexer, at the same time. This transistor sharing greatly reduces clock load and power consumption, while not compromising the performance.

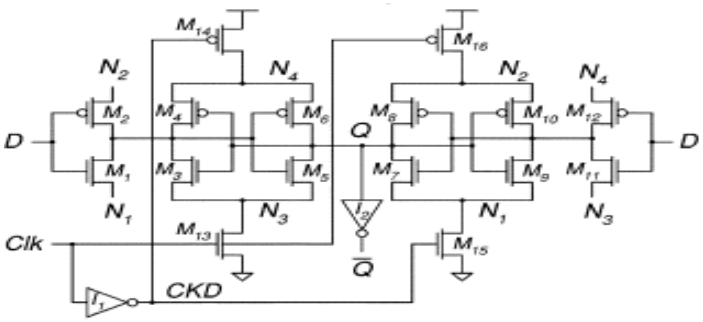

Fig.3: Transistor Diagram of a C2MOS LATCH-MUX

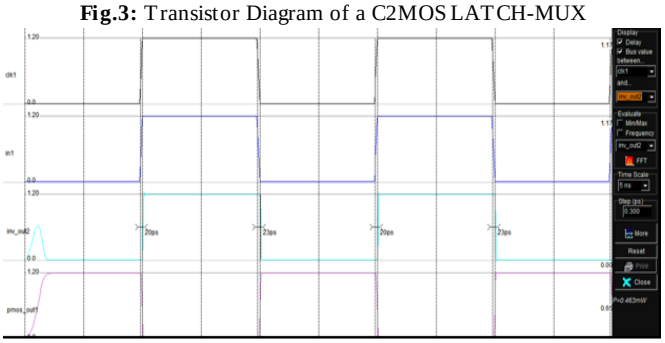

Fig.3: Simulation Wave form of a C2MOS LATCH-MUX

IV. DOUBLE EDGE CLOCK BRANCH SHARING IMPLICIT PULSED FLIP-FLOPS (CBS_IP):

The conventional DEFFs duplicate the area and the load on the inputs[1]. Explicit pulsed DEFFs use external clock pulse generators, which increase the power. In addition, explicit pulsed DEFFs cannot work with dynamic logic. SPGFF uses implicit pulsing; however, it has four internal redundant switching nodes. Unlike SPGFF, DECPFF eliminates the redundant switching activity, however, the number of clocked transistors reaches 21, and the clock branch duplicating structure is complex.

To ensure efficient implementation of double-edge clock triggering in an implicit pulsed environment and to overcome the problem with previous implicit pulsed flip-flops which is the large clock load, a novel clock branch sharing topology is used. The sharing concept is similar to the single transistor clocked FF and another clock branch sharing flip-flop. The advantage of this sharing concept is reflected in reducing the number of transistors required to implement the clocking branch of the double-edge triggered implicit-pulsed flip-flops. Without this sharing, the number of clocked transistors would be much larger than the number of transistors used with the sharing concept. Recall that clocked transistors consume a large amount of power. Reducing the number of clocked transistors is an efficient way to decrease the power. The CBS_ip uses the pseudo nMOS logic resulting from the conditional discharge technique.

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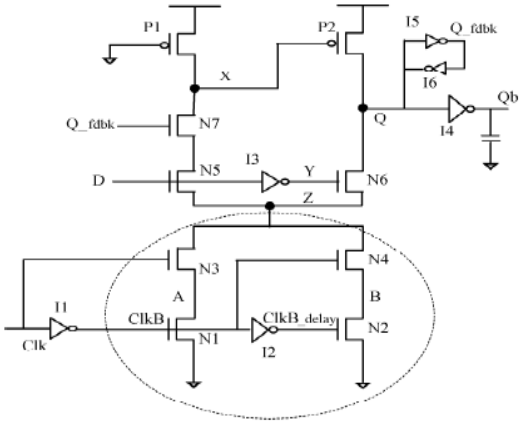

Fig.4: Transistor Diagram of CBS_IP DEFF

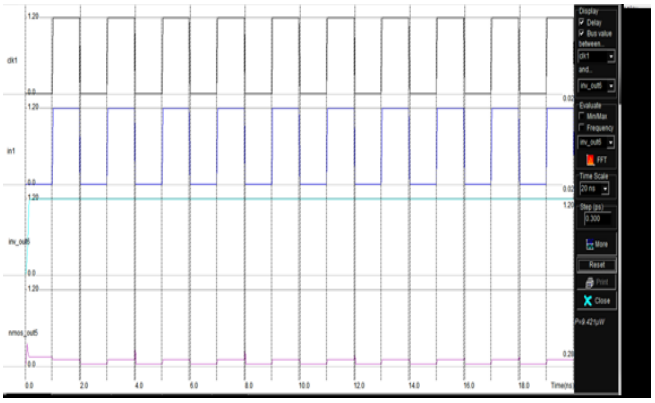

Fig.5: Simulation Wave form for CBS_IP DEFF

A. SHIFT REGISTER:

Shift registers are a type of sequential logic circuit, mainly for storage of digital data. They are a group of flip - flops connected in a chain so that the output from one flip - flop becomes the input of the next flip -flop. Most of the registers possess no characteristic internal sequence of states. All flip-flop is driven by a common clock, and all are set or reset simultaneously.

In these few lectures, the basic types of shift registers are studied, such as Serial In - Serial Out, Serial In - Parallel Out, Parallel In – Serial Out, Parallel In - Parallel Out, and bidirectional shift registers. A special form of counter - the shift register counter, is also introduced. A register that allows each of the flip -flops to pass the stored information to its adjacent neighbour.

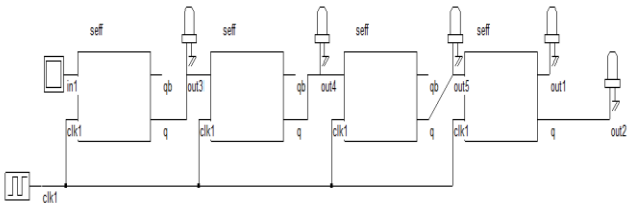

Fig.6: SISO Shift Register using SEFF

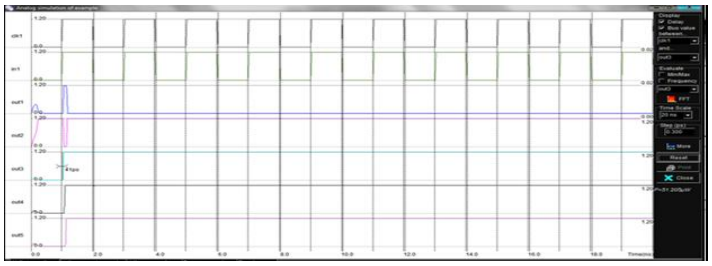

Fig.7: Simulation Wave form for Shift register

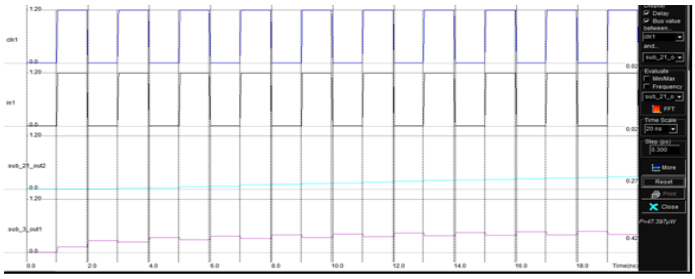

Fig.8: Simulation Wave form for DEFF C2MOS Latch MUX

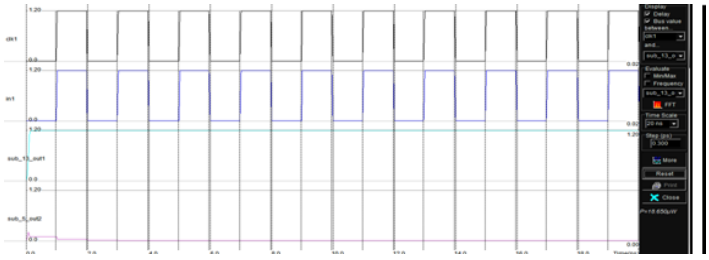

Fig.9: Simulation Wave form for Shift Register using CBS_IP

V. ADVANTAGES:

1. Number of transistors reduces
2. Delay is less
3. Power consumption reduces.

VI. APPLICATIONS:

1. Keyboard encoder
2. Multiplier
3. Micro processer
4. Micro controller

VII. ANALYSIS:

TABLE I

Comparison table

Name of the flip flops	No of transistors	Power consumption
Single edge triggering	28	51.82microwatts
Double edge triggering	18	47.6microwatts
Double edge triggering using cbs_ip	12	18.92microwatts

VIII. CONCLUSION

The simulation results are obtained for the designs of SEFF, C2MOS latch-MUX, CBS_ip DEFF and power consumption for the said designs are extracted from their corresponding output files and the comparisons are made in terms of number of transistors , and power consumption. Second it is designed 4 bit Serial- In-Serial-Out (SISO) shift registers for the designs C2MOS latch-MUX and CBS_ip DEFF and their outputs are verified. The performance is compared in terms of number of transistors and power consumption. It is compared from the results that, the power consumption is less for CBS_ip DEFF design as compared to C2MOS latch- MUX design.

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