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Basic Introduction to VLSI Technology with Processing Steps for Bipolar Junction Transistors: A Review

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ABSTRACT
In present electronics era, VLSI technology become is one of the most important and demandable theme. Behind this many reasons are presents include device portability, device size, large amount of features, cost, reliability, speed and many more. VLSI technology provides the suitability for designing electronics modules. In this paper we present the basic introduction of VLSI technology with processing steps or fabrication steps for bipolar junction transistors. We also described here, applications and uses of VLSI technology. With the help of this paper, one can easily understand the fabrication steps of BJTs and role of VLSI technology in present era.

Keywords:- SSI, MSI, LSI, VLSI, ULSI, GSI, ICs, Bipolar Junction Transistor, Oxidation, Photolithography, Diffusion, Epitaxy, Metallization.

I. INTRODUCTION

VLSI, the meaning of this word is Very Large Scale Integration or generally the term VLSI is also referred as Very Large Scale Integrated Circuit. At first we start here to understand the basic meaning of circuit. When we talking about circuits, a printed circuit board with different components like transistors, capacitors, resistors, diodes, connecting wires are comes in our mind. This is a type of discrete circuit where we use discrete components. In case of an integrated circuit the entire circuitry i.e. the active and passive elements everything is housed in the same substrate.

Depending on the circuit complexity of the integrated circuit we can classify it as SSI (Small Scale Integrated Circuit), MSI (Medium Scale Integrated circuit), LSI (Large Scale Integrated Circuit), VLSI (Very Large Scale Integrated Circuit), ULSI (Ultra Large Scale Integrated Circuit), and GSI (Giant Scale Integration/ Integrated Circuits. When we are talking about a circuit in which 10-100 transistors are housed in it then it is called small scale integrated circuit (example- flip-flops, gates) and when 100-1000 transistors are housed in any circuit then it is comes under medium scale integrated circuit (example- 4 bit microprocessors). More than 1000 (1000-10000) transistors circuits are come under large scale integrated circuit (example- 8-bit microprocessors, ROM, RAM). When the level of transistors are reached in high amount as 10000-1 millions of transistors housed in a small bit then these types circuits are called very large scale integrated circuits (example- 16-32 bit microprocessors). Ultra large scale integration technology is accommodated to the 1 million- 10 million amounts of transistors (example- special purpose registers). And when the level of transistors are reached in very high amounts as more than 10 million transistors housed in a small bit then this type circuits are called giant scale integrated circuit (example-embedded systems). Depending upon the manufacturing methods we can classify integrated circuits into three sub classes. First method is thin and thick film ICs, second method is monolithic ICs, and the third method is hybrid ICs. In thin or thick film integrated circuits transistors and diodes are connected as separate components but the passive components such as capacitor, resistors are integrated in circuit. In case of monolithic integrated circuits, the discrete components (active and passive) and interconnection, all things are formed on a silicon chip. That is the reason monolithic ICs are also called single stone ICs. In case of hybrid or multi chip ICs many chips are interconnected to each other. Generally metalized

pattern is used for providing interconnection between them. A general view of hybrid ICs is shown in figure 1.

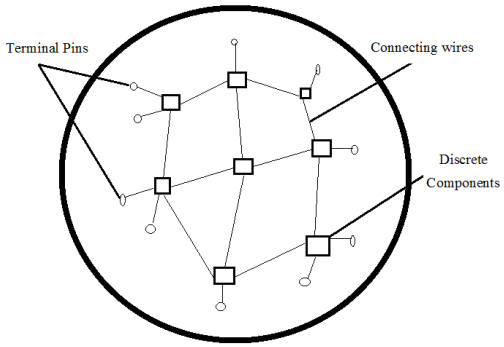

Figure 1- Hybrid ICs

In VLSI technology we discussed or learned about how these large amounts of transistors are fabricated in a circuit. What is the process behind it? VLSI technology is the answer of this question. Here first thing is that, in present time more than 95% of VLSI chips are made by silicon. Silicon is a group four elemental semiconductor. The most important element in an integrated circuit is its active element. The active elements are mainly classified in two terms (i)- Bipolar junction transistor (BJT), (ii)- Mattel-oxide semiconductor Field Effect Transistor (MOSFET). When we designed very high speed of circuits we usually use the BJTs and when we think about very high packaging density we usually use the MOSFETs. Hence we can say that VLSI technology is divided in two sub-categories one is BJTs based VLSI technology and another one is MOSFETs based VLSI technology. But as the increasing of transistors amount or increasing of the packaging density of the integrated circuits we also use the arrangement of these two technologies which brings about the new concept which is known as Bi-CMOS technology. It means we use in same circuit some active elements are bipolar junction transistors and some active elements are field effect transistors.

In this paper we present the basic processing steps of bipolar junction transistors. This gives the brief review for processing steps of BJTs. The paper is organized as follows: in Section II processing steps for bipolar junction transistors is reviewed. Subsequently, in section III, role of BJTs are presented. In section IV, advantages and uses of VLSI technology is presented. Finally a conclusion will be made in the last section.

II. PROCESSING STEPS FOR BIPOLAR JUNCTION TRANSISTORS

Basically BJT technology is older technology as compare to MOSFET technology. This is classified in two main subcategories one is NPN transistors and another one is PNP transistors. We start with P type single crystal oriented (1,1,1) and with a resistivity of 10 Ω cm., these are the most common starting substrate when we want to fabricate an NPN bipolar junction transistor. If we want to P type substrate then it means we want to dope it some mean of P type. So we use boron to dope in silicon. Boron is a group three element and silicon is a group four element therefore if we dope it in silicon we get P type substrate. In this case, the amount of boron which is used in doping must be carefully controlled because we want to relies a particular resistivity here 10 Ω cm., and this is the fact that the amount of dopent is controlled the resistivity of single crystal substrate. So we have identified the first processing step in VLSI technology which is crystal growth.

In crystal growth, the properties of crystal orientation are also plays important role. At first we have grown the crystal growth of (1,1,1) orientation. For integrated circuit fabrication we have the substrate material in wafer form it means very thin slice of block. Generally the slices are in disk form and their thickness will be a few hundred microns. The exact thickness will depend upon the diameter of the crystal. Right now we have a silicon substrate let us assume that we have managed to dope it P type also. We have realized a particular doping concentration so the resistivity of particular silicon wafer is 10 Ω cm., and if we see the cross-sectional view of this wafer it is like a simple rectangular shape shown in figure 2 and the three dimensional view of this is shown in figure 3.

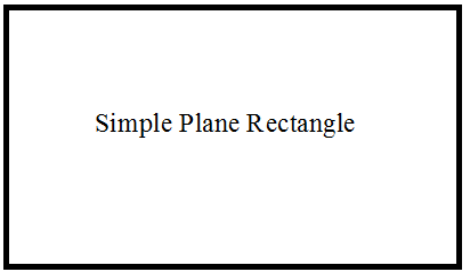

Figure 2-Cross sectional view of silicon wafer

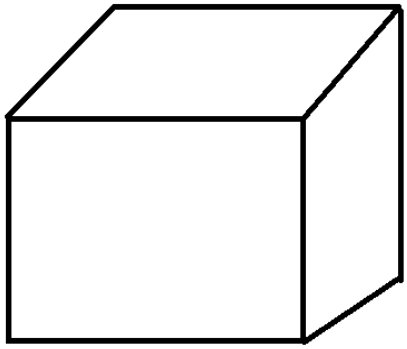

Figure 3- Three Dimensional View of Wafer

The next step after we have this silicon substrate for realizing the bipolar junction transistor is growing an oxide in entire silicon substrate. One of the best property of silicon material behind using this is that it is easily oxidized and after oxidation process it will formed in SiO_2 (Silicon die-oxide). This silicon die-oxide is an excellent insulating and dielectric material and it has also very good masking property. The meaning of masking property is that when we dope the silicon material we do not dope entire block of silicon we want to dope it selectively so the portion which we do not want to dope we covered that portion with the help of silicon die-oxide, silicon die-oxide will not allow to dope that portion or in other words we can say that it will work as a mask. Silicon die-oxide will mask against the doping. So silicon die-oxide has excellent insulating properties, dielectric properties, and masking properties which brings us next step namely the oxidation.

One we have oxidized the silicon substrate it looks like a transparent glass like layer on the single crystal substrate and it also shows different colour. Depending on the thickness of the oxide the colour will be blue, green or pink. An oxide layer is grown on the entire silicon substrate is shown in figure 4.

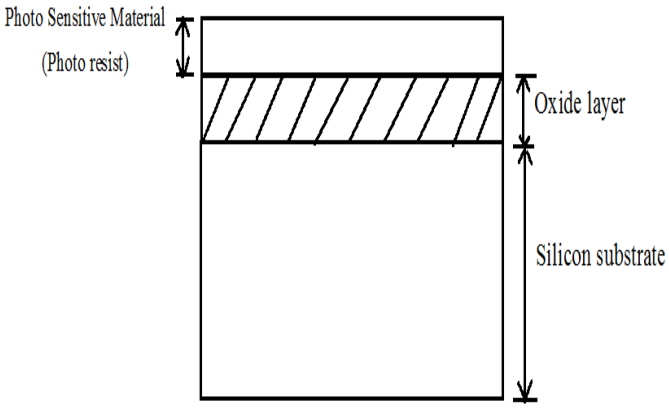

Figure 4-Oxide Layer Grown on Silicon Substrate

In figure 3 the entire surface of silicon substrate is covered with oxide layer. Once the entire substrate covered by oxide layer or silicon die-oxide, the next step is selectively dope the silicon substrate. When doping process happens, in that case we want to dope some reasons and also want to not dope regions wherever the oxide is presents it will act as a mask against doping and where we remove oxide it will be called doped regions. This selective removal of oxide is done by a special technique called photolithography. So photolithography is our third step for fabrication. In this step we covered the entire surface of oxidized silicon with a photosensitive material. The photosensitive material is called a photo resist. Photo resist is a light sensitive material. Silicon substrate covered by photo resist is shown in figure 5.

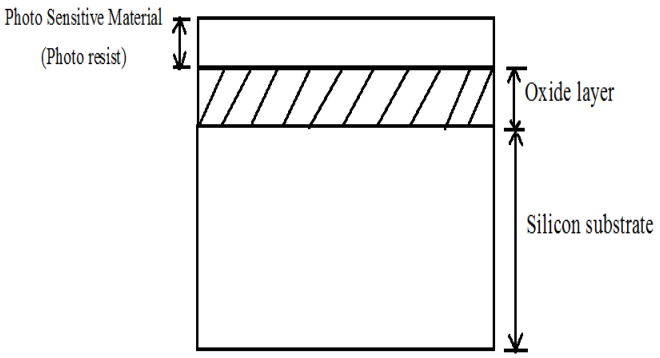

Figure 5- Silicon Substrate Covered by Oxide layer and Photo Resist

At first we put this photosensitive material or photo resist on the entire substrate then we bring this photo resist coated substrate in contact with a mask. Mask is a simple glass plate with patterns. Then we subject it to a particular radiation. U-V radiation is most commonly used

radiations. We know that photo resist is a light sensitive material so through the transparent radians of the mask this photo resist is exposed to the U-V light radiations and it properties changed it become soft or easy to remove those portions. And in rest portion the photo resist is hard and it is difficult to remove so it is going to protect the underline oxide layer. The object is shown after this process is just like as figure 6.

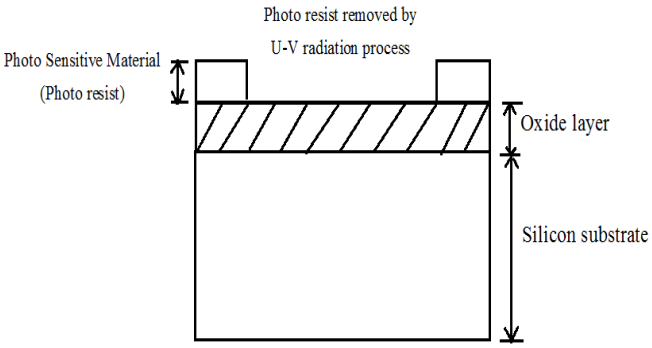

Figure 6- Object after U-V Radiation Process

And then our subject is to etching, for etching of oxide we put it in hydrofluoric acid solution which can etch silicon die-oxide while preserving a silicon substrate. So when this is put in hydrofluoric acid solution only oxide portion will remove. The new object structure after this process is shown in figure 7.

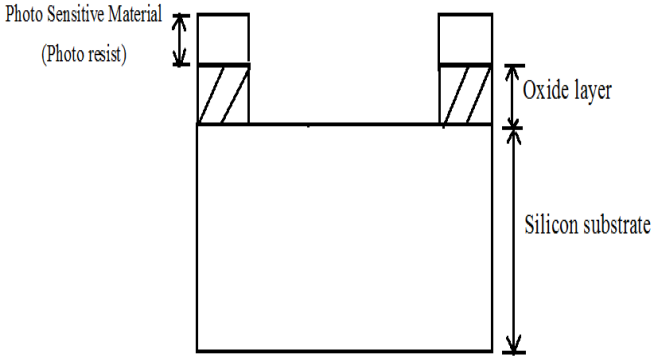

Figure 7- Object after Deep in Hydrofluoric Acid

And then we can remove the remaining photo resist from the rest of the portions. This term is called opening of a window in the oxide. We have opened a window in the oxide. New structure is shown in figure 8.

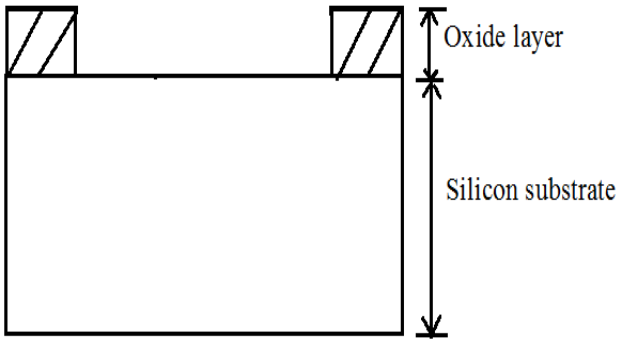

Figure 8- Object after window opening

So now that to open this window in the oxide, the mask we needed is something like a square cut transparent window while rest of portion is on dark. This is shown in figure 9.

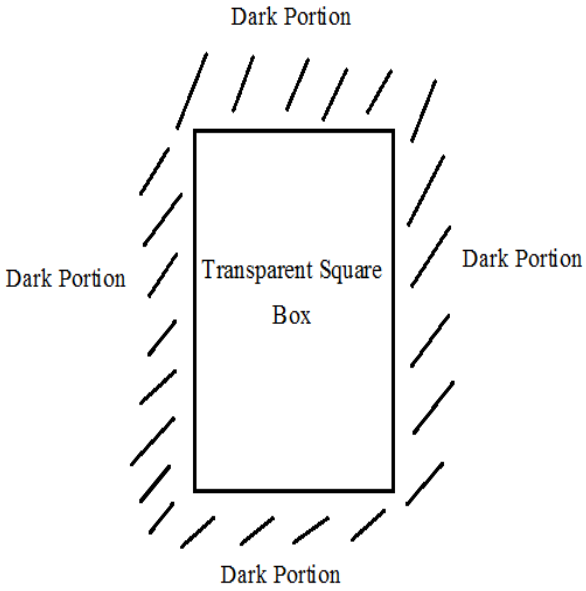

Figure 9- Top View of Mask

So only through this transparent square the photo resist is exposed to the U-V radiation, it get soften and easy to remove. This mask incidentally is called the active layer mask in bipolar junction transistors it means that this is the active region where the transistors will actually be housed.

Hence we can say that photolithography is closely related to photo resist, masks, and radiations.

After we have realized this window pattern the next step will be to dope through the window (the region where the oxide is not present) and we usually do diffusion

process (N^+) (N^+ is very heavily doped N region). So diffusion is our next process step.

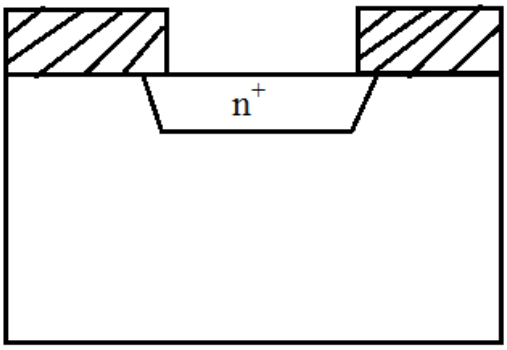

Figure 10- Object with n^+ diffusion

This particular diffusion incidentally is called buried layer diffusion. This N^+ layer diffusion usually the dopent used for this is antimony or arsenic. After the buried layer diffusion we remove rest part of the oxide. So the structure is like figure 11.

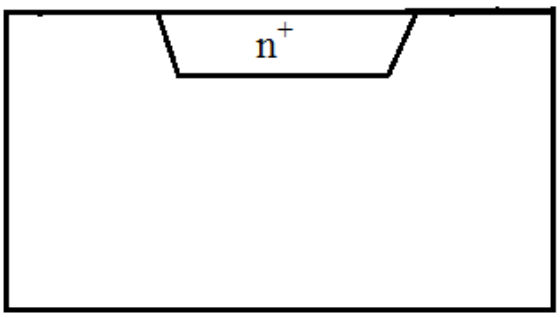

Figure 11- Object without Rest Part of Oxide

Now we have a buried silicon substrate, in the active region it is doped n^+. The next step is called epitaxy. The meaning of epitaxy means arranged a new upper layer. We have a single crystal substrate layer and we also go to arrange a single crystal layer upon this layer. With the help of epitaxy process we will go to grow a n layer on top of this substrate. While growing this n layer the n^+ layer diffuses layer out of this and the structure looks like figure 12.

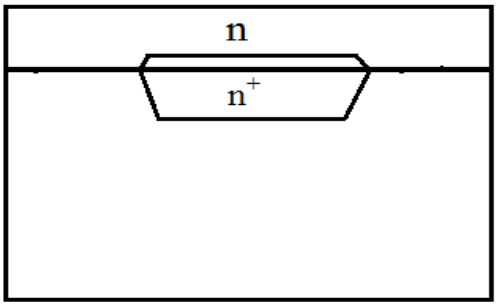

Figure 12- Object with Grow n layer

Now in figure 11 it is clear that the n^+ layer is buried with n epitaxial layer. Now we have a p type substrate, n^+ buried layer diffusion and on the top n epitaxial layer. This in epitaxial layer is going to be the collector of the n-p-n transistor and the n^+ buried layer diffusion is done in order to reduce the collector resistance. Now this n epitaxial layer is going to be the collector of the bipolar junction transistor, obviously we are not going to have just one transistor in this entire silicon chip, we are going to have thousands of transistors. The collectors are shorted together because all of them are housed in the same epitaxial region. We do not want this condition. Because we do not know what kind of circuit we made, if we were making discrete transistors then this problem is not come in front of us because we cut individual transistor, but in case of integrated circuit everything such as passive components, interconnections, active components etc. is housed in the same chip then we can't allow that all the collectors are shorted together. So this is one important criteria of integrated technology that is to provide isolation between adjacent devices. So we must concentrate the scheme to adjacent the devices. The oldest technology for isolation between transistors, use is a reverse bias p-n junction. We know a reverse bias p-n junction is a blocking contact. It's not allows the flow of current between two transistors. In this case we generally call this process p-n junction isolation. In this process we protect the active region by means of an oxide and dope by p^+ diffusion. In this process it is very important that this doping (p^+) comes all the way to the p type substrates. Then we get that our transistor are isolated to each other. This process is shown in figure 13.

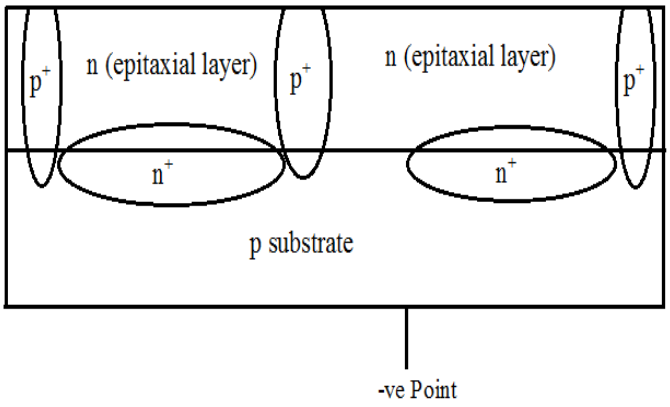

Figure 13- Isolation between Transistors Through p-n junction Isolation

In this figure we can clearly see that two transistor are isolated from each other through reversed bias p^+ junction it means current can not flow through this reverse bias p^+ junction. One main thing in this process is that the substrate is connected to the most –ve point of the supply. This process is called p-n isolation. The main precaution point of this process is that the selectivity diffused this p^+ region. The top view of mask for this p^+ region is shown in figure 14.

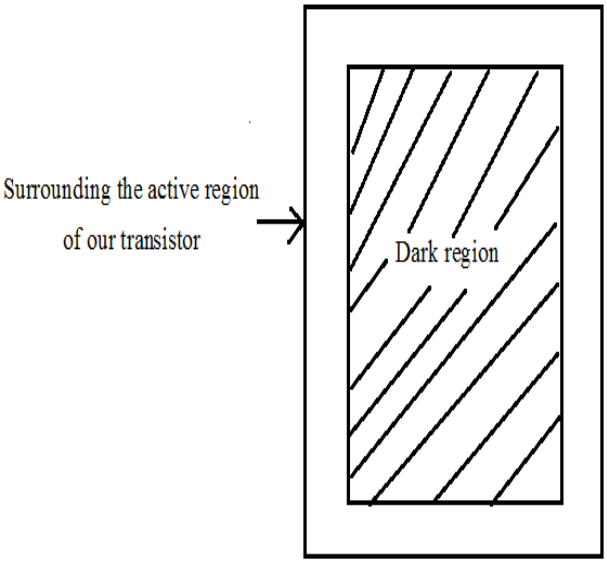

Figure 14- Top view of the Mask for p^+ Region

Figure 14 tells us that the p^+ dopent enter only through outer region or surrounding the active region of our transistor. The active region is marked by n^+ berried layer diffusion. So right now we realize the collector. And our next task is to realize the base and emitter. The base is doped earlier then emitter because the emitter is more highly doped as compare to the base. So at first we will concentrate on base doping. For this purpose all we have to do now is to have a p region. P region used doping for the base. This is shown in figure 15.

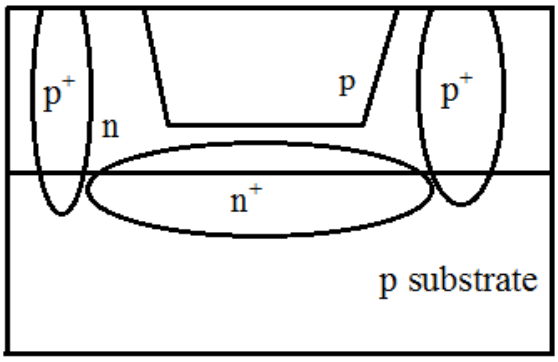

Figure 15- Doping for Base Realization

In order to realize a p region is oxidation, photolithography, and diffusion. These all three process are used almost in every stage processing or in other words we can say that these three process step are repeated. The base region is located within the active region mask. The top view is this is shown in figure 16.

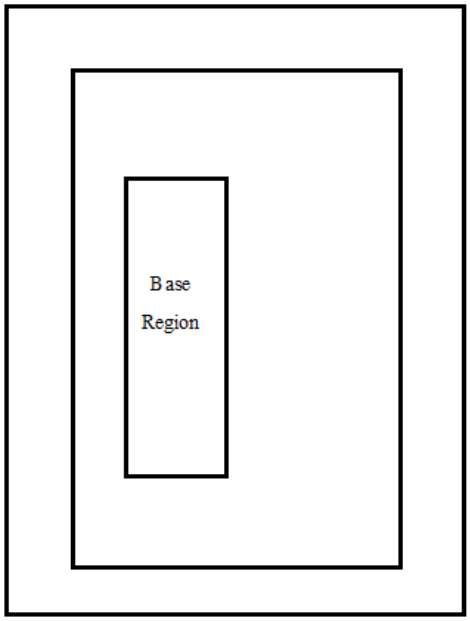

Figure 16- Top View of Mask after Base Realization

In figure 16, base is actually located within the active region mask, only base region will be transparent when we

are going to have the mask for the base. So we have realized the base. Now we will focus on the realization of emitter. Within the base window we have the emitter region. The object view and top view of this realization is shown in figure 17 and 18 respectively.

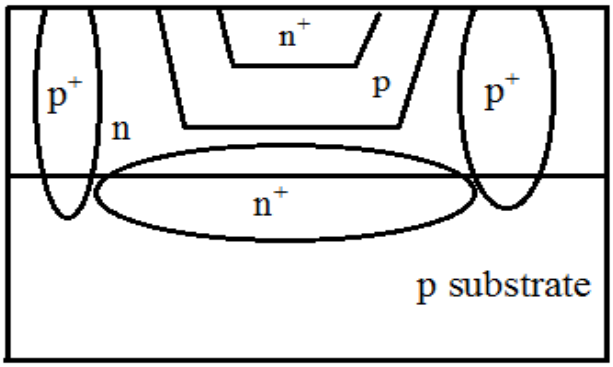

Figure 17-Doping for Emitter Realization

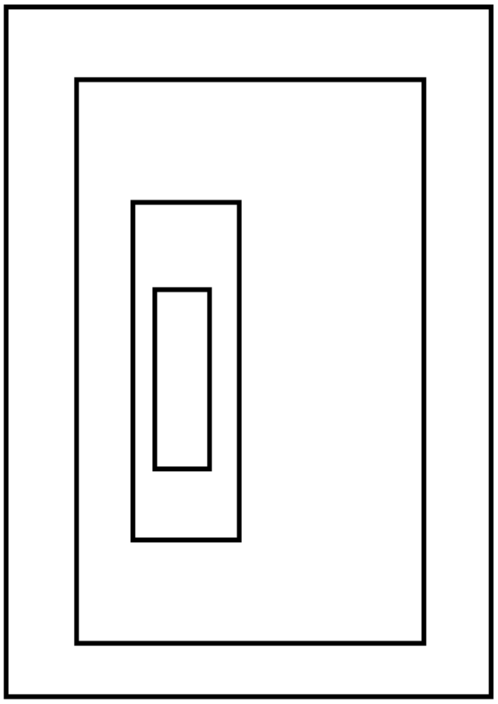

Figure 18-Top View of Mask after Emitter Realization

When we are going for emitter doping we also have a small n region in order to facilitate taking contact from the collator region. In figure our collator is n, this is epitaxial n region, it is not very heavily doped, it is lightly doped n region. So in order to take contact from that lightly doped n region we want to reduce contact resistance it is difficult to have a proper ohmic contact to a lightly doped n region. So the usual practice is we have a small pocket of n^+ diffusion for collector contact. This small pocket for collector contact is shown in figure 19. This needs no extra step. This can be done along with the emitter diffusion. The top view of this is shown in figure20.

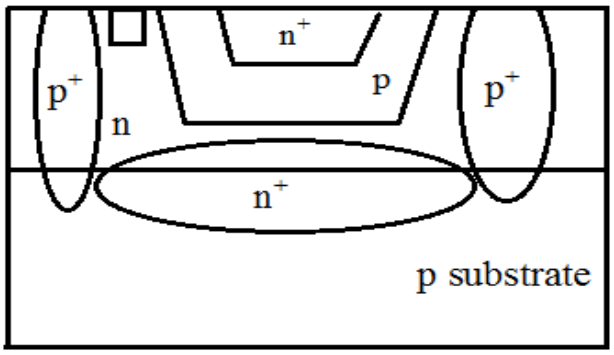

Figure 19- N^+ Diffusion for Collector Contact (Small Pocket)

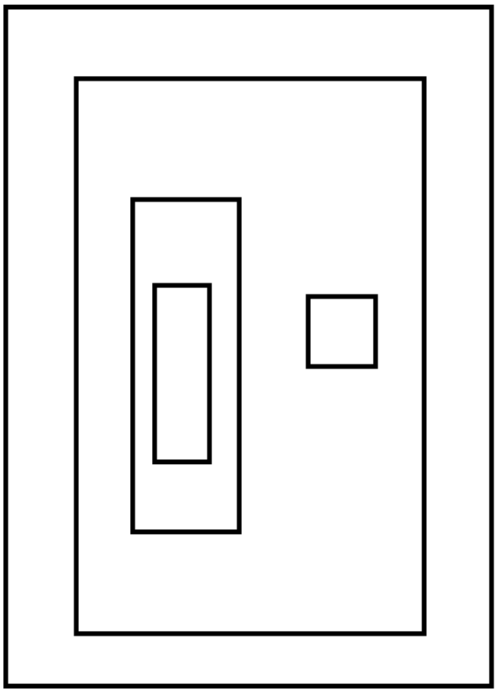

Figure 20-Top View of Mask with Small Pocket

This pocket box is present inside the active region.

So the transistor is almost ready we have realized the emitter, base, collector, and isolation between adjacent devices. The remaining part of this process is to establish the contact with the outside world. This is done by a technique is called contact metallization. This metallization needs selective deposition of metal over the base, emitter and collector region. That is when we use the term of selective we take help for this by using

photolithography process. Because for this purpose we also must have masks. The contact diagram is shown in figure 21. The aluminum material is used usually for contacting purpose in VLSI. Aluminum is also a group three element it means aluminum would actually dope silicon p type. So when we are contacting in p region the use of aluminum is very easy. The aluminum makes it p^+ therefore the contact resistance is going to be very small. The situation is very tuff when we have a n region, however if we have a heavily doped n^+ region it's not a problem because it is good enough for ohmic contact. The only problem when we have lightly doped n region so for the solution purpose we use a n^+ pocket for taking collector contacts. The latest technology for contacting material is use of copper because aluminum has also some problems like electro migration and many others.

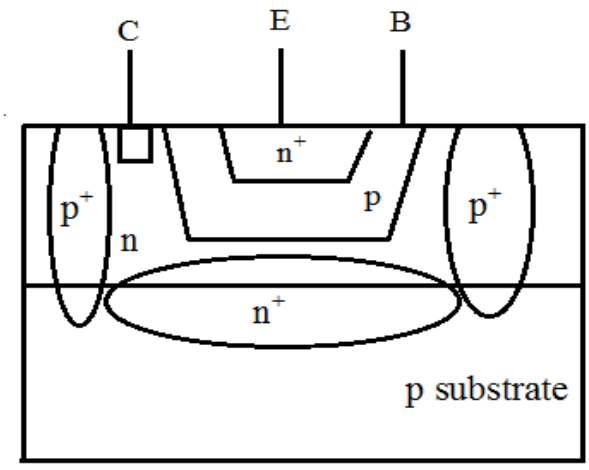

Figure 21-Contact Diagram of Final Transistor

For metallization process we will also require masks which are shown in figure 21, the top view of this.

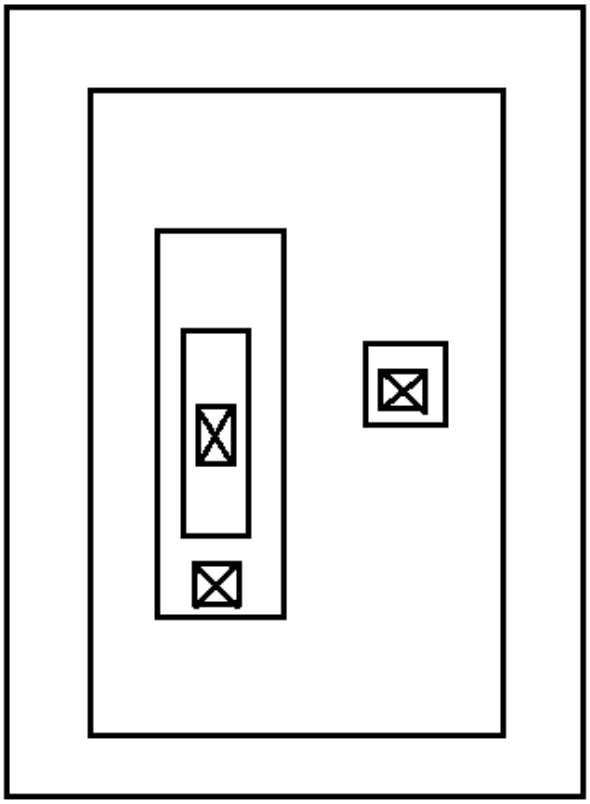

Figure 22- Top view of Mask for Metallization Purpose

So these are the simple steps we need to realize a bipolar junction transistor. The simple flow of these steps is shown in figure 23.

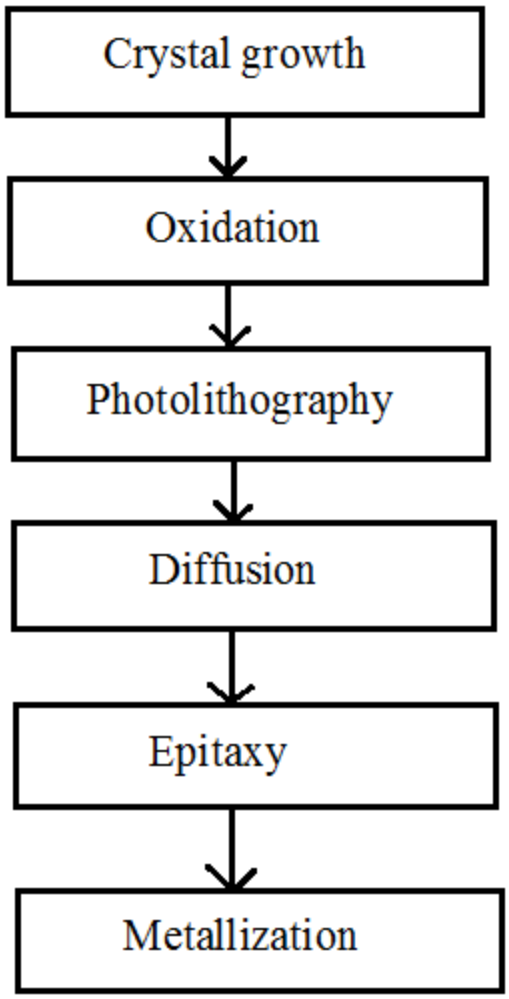

Figure 23- Flow of Processing Steps for Realizing Bipolar Junction Transistors

III. ROLE OF BJTS IN ELECTRONICS

Mainly there are two types of uses of BJTs one is switching and another one is amplification. When transistor is biased to operate cutoff or saturation region then it will works as a switching application. When the cut-off region, transistor will act as open switching, and when saturation region, it will act as closed switching. The trans-conductance and output resistance of BJTs is high then MOSFETs, so it is used for designing in many discrete circuits. In case of high frequency applications BJTs are also provides suitability. That's the reason BJTs are used in wireless systems for radio frequency. BJTs are also used in metal proximity photocells. The working mode of BJTs as also classified in three terms one is common base mode, second one is common emitter mode, and third one is common collector mode. BJTs are classified in two sub classes based on their working flow. First is NPN transistor and second is PNP transistor. The circuit symbol of NPN and PNP transistor is shown in figure 24, 25 respectively. The meaning of NPN and PNP is generally 'Never points in', and 'Points in permanently' respectively.

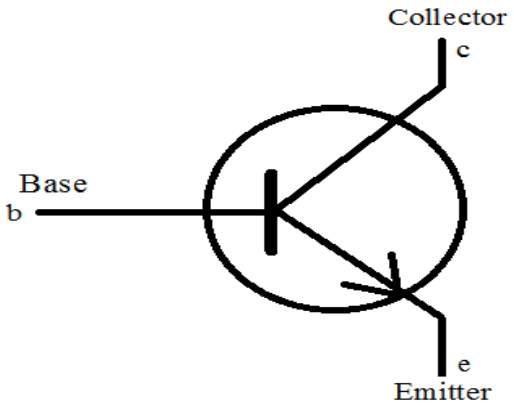

Figure 24- Circuit Symbol of NPN Transistor

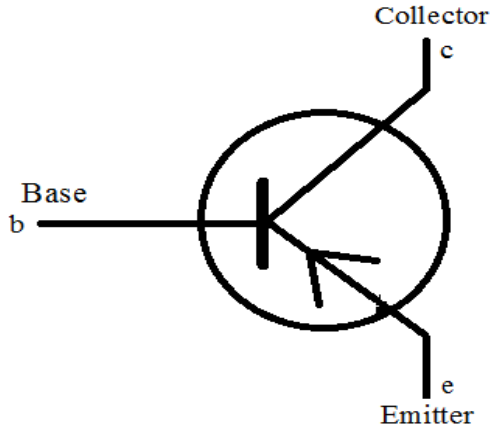

Figure 25- Circuit Symbol of PNP Transistor

IV: Advantages and Uses of VLSI technology

There are lots of advantages of VLSI technology. These are, portability (its provides the smart and portable and compact devices with less weight), high operating speed, less power consuming devices, good reliability, cost effective, environmental viewpoint and many more [1].

In present time VLSI technology is used in various fields includes digital image processing applications for improving the vision standards, image data transmissions, image restoration, segmentation [2-15], medical research applications and circuit designing for analysis of hard medical problems [16-20], wireless communication applications [21-22], nano technology based applications and many more. VLSI technology also plays role in many research areas as aerospace, satellite, communication etc. The demand of VLSI technology increasing day by day because almost electronics devices and instruments are based on this technology and VLSI technology also introduce a special term named low power VLSI [1], by using this term designer increased their device performance and cost.

IV. CONCLUSION

In this paper we present the basic introduction of VLSI technology with classification of circuits in term of their complexity. We described in this paper the importance of VLSI technology, i.e. how much this technology is important in present era. We also present in this paper the basic processing steps for bipolar junction transistors and their role in electronics. One can easily understand the importance of VLSI technology and processing steps for BJT with the help of this paper.

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